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MC68HC11EA9
MC68HC711EA9

Technical Summary
8-Bit Microcontrollers

1 Introduction

The MC68HC11EA9 and MC68HC711EA9 microcontroller units (MCUs) are high-performance members of the M68HC11 family of MCUs. The MC68HC(7)11EA9 MCUs have a multiplexed external address and data bus and are characterized by high speed and low power consumption. Their fully static design allows operation at frequencies from 3 MHz to dc. The addition of a phase-locked loop (PLL) frequency synthesizer to the timer circuitry further enhances low-power operation and allows the use of lower frequency crystals while maintaining a clock speed of up to 3 MHz.

This document contains information concerning standard and custom-ROM devices. Standard devices are those with ROM or with EPROM replacing ROM (MC68HC711EA9). Custom-ROM devices have a ROM array that is programmed at the factory to customer specifications. Where information in this document refers to both the ROM and EPROM versions, the device is referred to as MC68HC(7)11EA9.

1.1 Features

- M68HC11 CPU
- 512 Bytes RAM (Data Retained During Standby, by use of V_{STBY})
- 12 Kbytes Mask-Programmed ROM or EPROM
- 512 Bytes Electrically Erasable Programmable ROM (EEPROM)
- PROG Mode Allows Use of Standard EPROM Programmer (27C256 Footprint)
- Multiplexed Address and Data Buses Reduce Pin Count
- Enhanced 16-Bit Timer with Four-Stage Programmable Prescaler
  - — Three Input Capture (IC) Channels
  - — Four Output Compare (OC) Channels
  - — One Additional Channel, Selectable as Fourth IC or Fifth OC
- 8-Bit Pulse Accumulator
- Phase-Locked Loop (PLL) Frequency Synthesizer for Reduced Power Consumption
- Power Saving STOP and WAIT Modes
- Real-Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog Timer
- Clock Monitor Circuit
- Enhanced Asynchronous Nonreturn to Zero (NRZ) Serial Communications Interface (SCI)
- Eight-Channel 8-Bit Analog-to-Digital (A/D) Converter
- Five Input/Output (I/O) Ports (34 Pins)
  - — Four Bidirectional I/O Ports (26 Pins)
  - — One Fixed Input-Only Port (8 Pins)
- Two Alternate, Fixed Input-Only Pins ($\overline{XIRQ}$ pin/XPIN bit and $\overline{IRQ}$ pin/IPIN bit)
- Available in 52-Pin Plastic Leaded Chip Carrier (PLCC), 52-Pin Windowed Ceramic Leaded Chip Carrier (CLCC), and 56-Pin SDIP (0.070” Lead Spacing)

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TOC1–TOC4	Timer Output Compare	$1016–$101D	42

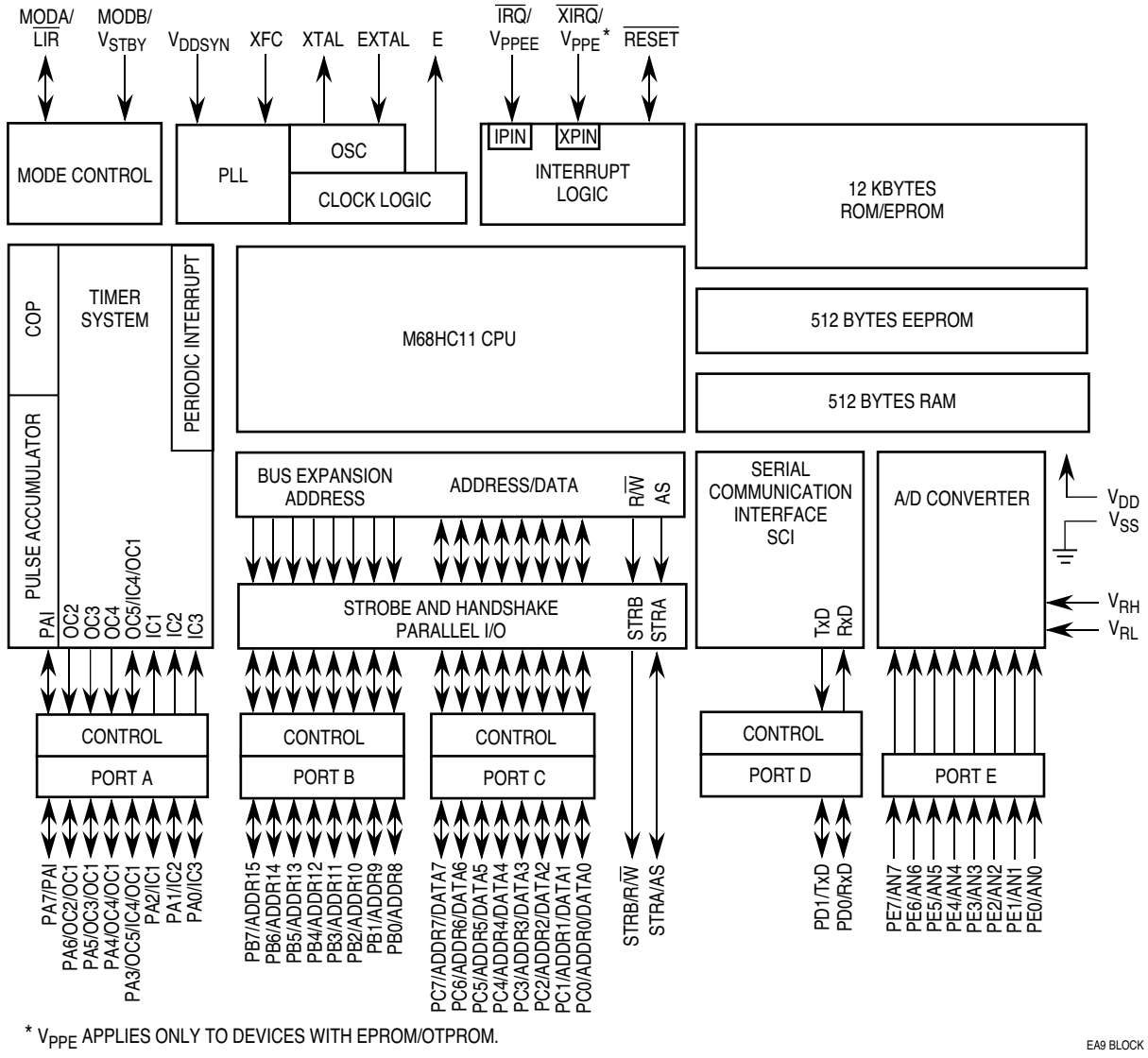


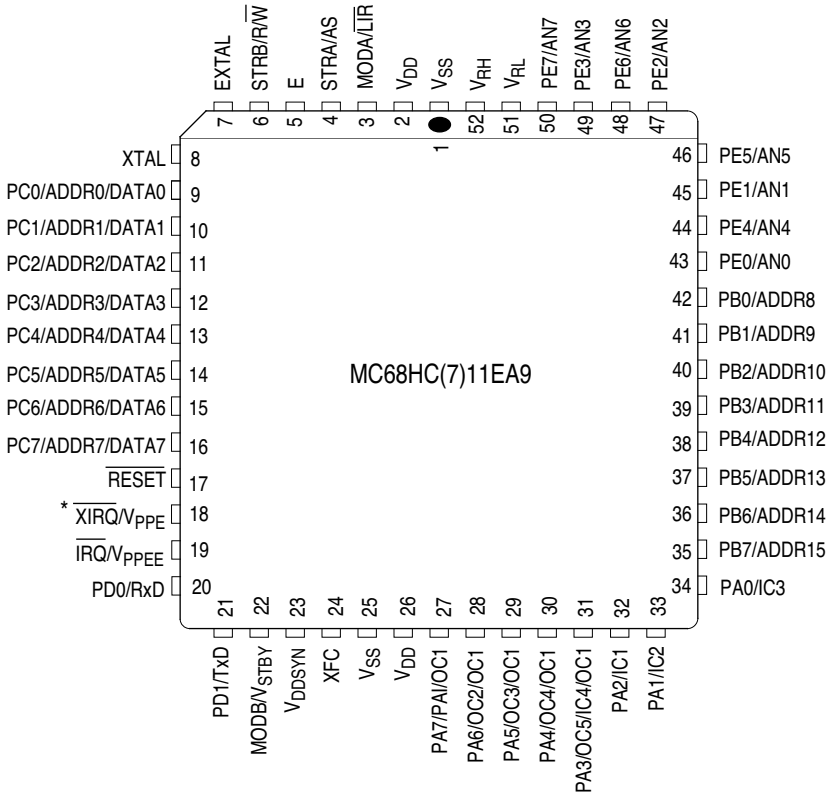
Figure 1 MC68HC(7)11EA9 Block Diagram

2 Device Package Options and Ordering Information

2.1 Available Device Packages

The MC68HC(7)11EA9 MCUs are available in a 52-pin plastic leaded chip carrier (PLCC) and a 52-pin ceramic leaded chip carrier (CLCC). Refer to **Figure 2**. A plastic 56-pin shrink DIP (SDIP) package is also available. Refer to **Figure 3**.

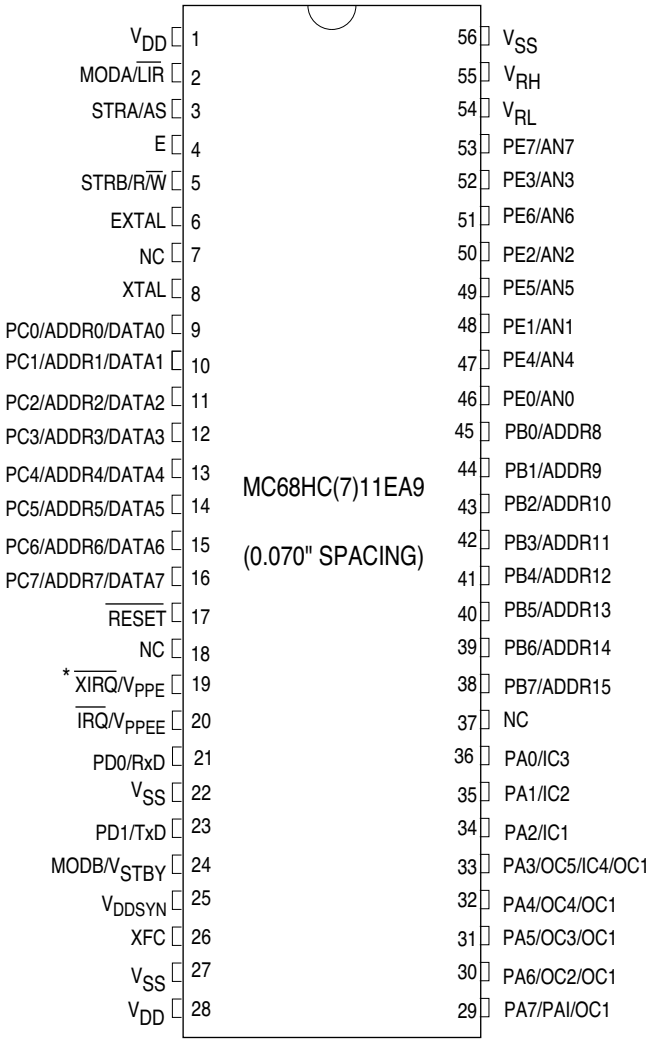
The EPROM-based MC68HC711EA9 is available in a windowed 52-pin ceramic leaded chip carrier (CLCC). A one-time-programmable (OTP) version of the MC68HC711EA9 is available by ordering the device in a non-windowed package. Refer to **Table 1**.



* V_{PPE} APPLIES ONLY TO DEVICES WITH EPROM/OTPROM.

EA9 52-PIN PLCC

Figure 2 MC68HC(7)11EA9 PLCC/CLCC Pin Assignments



* V_{PPE} APPLIES ONLY TO MC68HC711EA9.

EA9 56-PIN DIP

Figure 3 MC68HC(7)11EA9 56-Pin SDIP Pin Assignments

2.2 Ordering Information

The MC68HC(7)11EA9 MCUs are available in a combination of packages, speeds, and temperature ranges. Refer to **Table 1**.

Table 1 Device Ordering Information

Description	Package	Temperature	Frequency	MC Order Number
Buffalo ROM	52-Pin PLCC	– 40° to + 85° C	2 MHz	MC68HC11EA9BCFN2
12 Kbytes ROM, 512 Bytes RAM			2 MHz	MC68HC11EA9CFN2
			3 MHz	MC68HC11EA9CFN3
		– 40° to + 105° C	2 MHz	MC68HC11EA9VFN2
			3 MHz	MC68HC11EA9VFN3
		– 40° to + 125° C	2 MHz	MC68HC11EA9MFN2
			3 MHz	MC68HC11EA9MFN3
	56-PIN SDIP (.070” Spacing)	– 40° to + 85° C	2 MHz	MC68HC11EA9CP2
			3 MHz	MC68HC11EA9CP3
		– 40° to + 105° C	2 MHz	MC68HC11EA9VP2
			3 MHz	MC68HC11EA9VP3
		– 40° to + 125° C	2 MHz	MC68HC11EA9MP2
			3 MHz	MC68HC11EA9MP3
12 Kbytes OTPROM, 512 Bytes RAM	52-Pin PLCC	– 40° to + 85° C	2 MHz	MC68HC711EA9CFN2
			3 MHz	MC68HC711EA9CFN3
		– 40° to + 105° C	2 MHz	MC68HC711EA9VFN2
			3 MHz	MC68HC711EA9VFN3
		– 40° to + 125° C	2 MHz	MC68HC711EA9MFN2
			3 MHz	MC68HC711EA9MFN3
	56-PIN SDIP (.070” Spacing)	– 40° to + 85° C	2 MHz	MC68HC711EA9CP2
			3 MHz	MC68HC711EA9CP3
		– 40° to + 105° C	2 MHz	MC68HC711EA9VP2
			3 MHz	MC68HC711EA9VP3
		– 40° to + 125° C	2 MHz	MC68HC711EA9MP2
			3 MHz	MC68HC711EA9MP3
12 Kbytes EPROM, 512 Bytes RAM	52-PIN CLCC (Windowed)	– 40° to + 85° C	2 MHz	MC68HC711EA9CFS2
			3 MHz	MC68HC711EA9CFS3
		– 40° to + 105° C	2 MHz	MC68HC711EA9VFS2
			3 MHz	MC68HC711EA9VFS3
		– 40° to + 125° C	2 MHz	MC68HC711EA9MFS2
			3 MHz	MC68HC711EA9MFS3

3 Central Processing Unit

A full description of the CPU and instruction set of M68HC11 MCUs is beyond the scope of this summary. The programming model for the M68HC11 CPU and a brief description of the CPU registers is provided here. For more detailed information refer to the *M68HC11 Reference Manual* (M68HC11RM/AD) or the programming reference guide or technical data book for the appropriate device.

3.1 Programming Model

Figure 4 shows a graphic representation of the internal registers of the M68HC11 CPU.

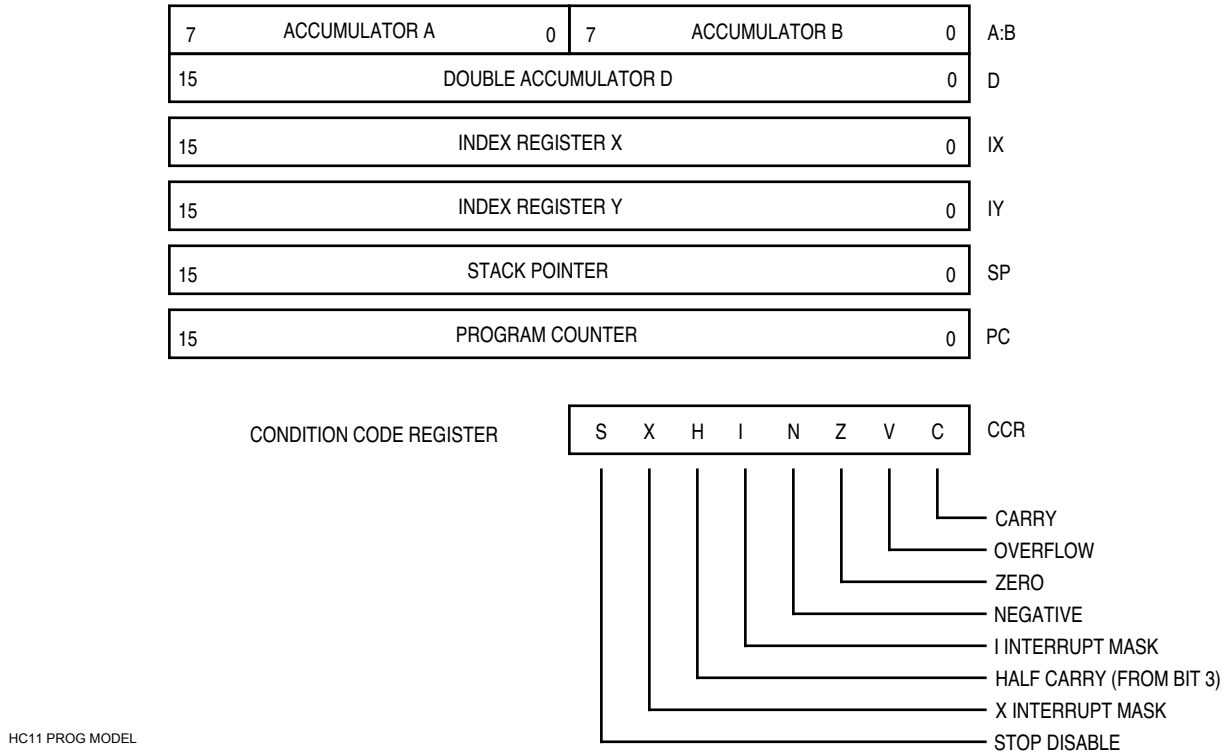


Figure 4 M68HC11 Programming Model

3.2 CPU Registers

M68HC11 CPU registers are an integral part of the CPU and are not addressed as if they were memory locations. The seven registers, discussed briefly in the following paragraphs, are shown in **Figure 4**. For a complete description of the CPU registers, addressing modes, and instruction set refer to the *M68HC11 Reference Manual* (M68HC11RM/AD).

3.2.1 Accumulators A, B, and D

Accumulators A and B are general-purpose 8-bit registers that hold operands and results of arithmetic calculations or data manipulations. For some instructions, these two accumulators are treated as a single double-byte (16-bit) accumulator called accumulator D. Most instructions can use accumulators A or B interchangeably, however some exceptions apply.

3.2.2 Index Register X (IX)

The IX register provides a 16-bit indexing value that can be added to the 8-bit offset provided in an instruction to create an effective address. The IX register can also be used as a counter or as a temporary storage register.

3.2.3 Index Register Y (IY)

The 16-bit IY register performs an indexed mode function similar to that of the IX register. However, most instructions using the IY register require an extra byte of machine code and an extra cycle of execution time because of the way the opcode map is implemented.

3.2.4 Stack Pointer (SP)

The M68HC11 CPU has an automatic program stack. This stack can be located anywhere in the address space and can be any size up to the amount of memory available in the system. Normally the SP is initialized by one of the first instructions in an application program. The stack is configured as a data structure that grows downward from high memory to low memory. Each time a new byte is pushed onto the stack, the SP is decremented. Each time a byte is pulled from the stack, the SP is incremented. At any given time, the SP holds the 16-bit address of the next free location in the stack.

3.2.5 Program Counter (PC)

The program counter, a 16-bit register, contains the address of the next instruction to be executed. After reset, the program counter is initialized from one of six possible vectors, depending on operating mode and the cause of reset.

3.2.6 Condition Code Register (CCR)

This 8-bit register contains five condition code indicators (C, V, Z, N, and H), two interrupt masking bits, ($\overline{\text{IRQ}}$ and $\overline{\text{XIRQ}}$) and a stop disable bit (S). In the M68HC11 CPU, condition codes are automatically updated by most instructions. For example, load accumulator A (LDAA) and store accumulator A (STAA) instructions automatically set or clear the N, Z, and V condition code flags.

3.2.7 Addressing Modes

Six addressing modes can be used to access memory: immediate, direct, extended, indexed, inherent, and relative. These modes are not detailed in this manual. For a complete description of the CPU registers, addressing modes, and instruction set refer to the *M68HC11 Reference Manual* (M68HC11RM/AD).

4 Operating Modes and On-Chip Memory

4.1 Single-Chip Mode

In single-chip mode, ports B and C are available for general-purpose parallel I/O. Strobe pins A (STRA) and B (STRB) can be used to control handshaking of parallel I/O on ports B and C. In this mode, all software needed to control the MCU is contained in internal resources. ROM/EPROM (if present) will always be enabled out of reset, ensuring that the reset and interrupt vectors will be available at locations $FFC0–$FFFF.

4.2 Expanded Mode

In expanded operating mode, the MCU can access the full 64-Kbyte address space. The space includes the same on-chip memory addresses used for single-chip mode as well as addresses for external peripherals and memory devices. The expansion bus is made up of ports B and C, and control signals AS and R/$\overline{W}$. R/$\overline{W}$ (read/write) and AS (address strobe) allow the low-order address and the 8-bit data bus to be multiplexed on the same pins. During the first half of each bus cycle address information is present. During the second half of each bus cycle the pins become the bidirectional data bus. AS is an active-high latch enable signal for an external address latch. Address information is allowed through the transparent latch while AS is high and is latched when AS drives low. **Figure 5** shows an example of address and data demultiplexing.

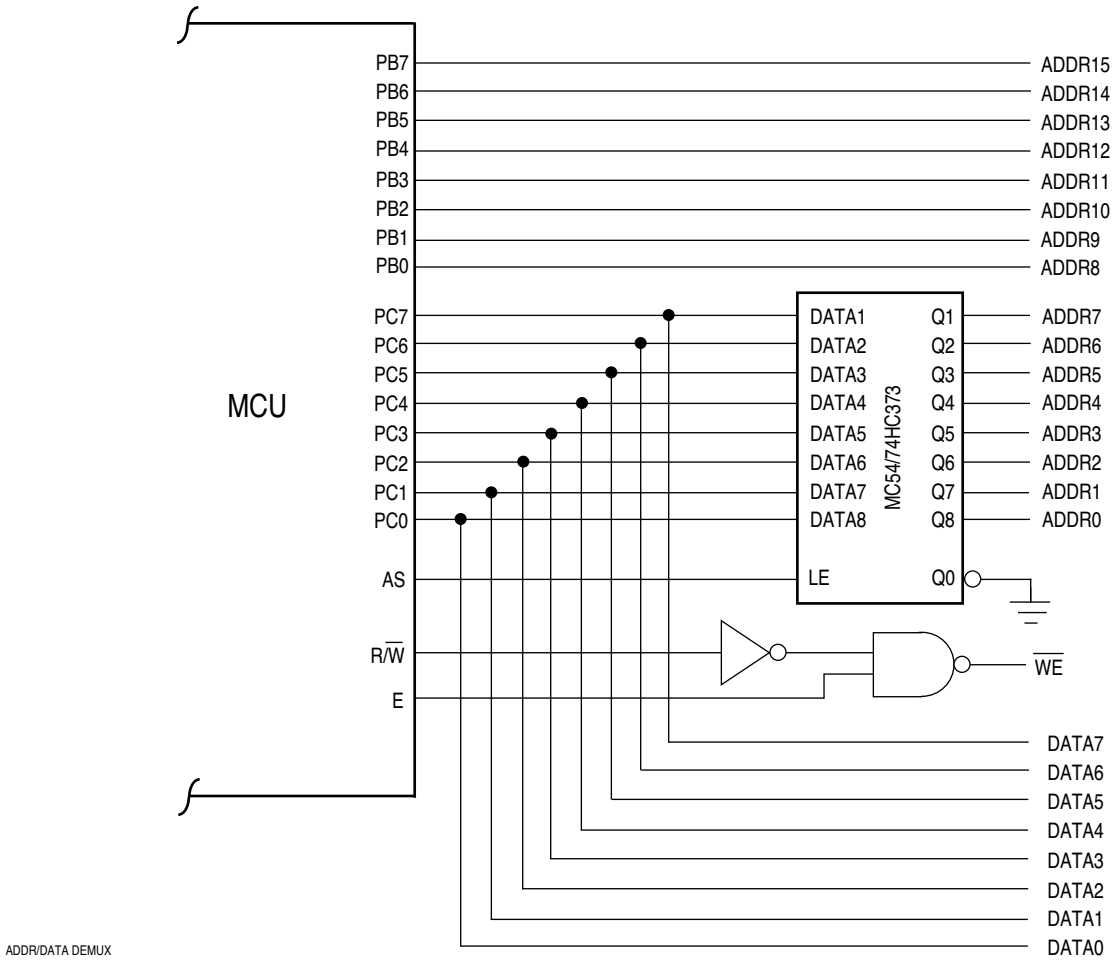


Figure 5 Address/Data Demultiplexing

4.3 Test Mode

Test mode, a variation of the expanded mode, is primarily used during Freescale's internal production testing; however, it is accessible for programming the CONFIG register, programming calibration data into EEPROM, and supporting emulation and debugging during development. Refer to **Figure 6**.

4.4 Bootstrap Mode

Bootstrap mode is a special variation of the single-chip mode. Bootstrap mode allows special-purpose programs to be entered into internal RAM. When boot mode is selected at reset, a small bootstrap ROM becomes present in the memory map. Reset and interrupt vectors are located in this ROM at $BFC0–$BFFF. The bootstrap ROM contains a small program which initializes the SCI and allows the user to download a program into on-chip RAM. The size of the downloaded program can be as large as the size of the on-chip RAM. After a four-character delay, or after receiving the character for the highest address in RAM, control passes to the loaded program at $0000. Refer to **Figure 6**.

4.5 Mode Selection

The four mode variations are selected by the logic levels present on the MODA and MODB pins during reset. The MODA and MODB logic levels determine the logic state of SMOD and the MDA control bits in the highest priority I-bit interrupt and miscellaneous (HPRIO) register. See **Table 2** for further information.

After reset is released, the mode select pins no longer influence the MCU operating mode. In single-chip operating mode, the MODA pin is connected to a logic level zero. In expanded mode, MODA is normally connected to V_{DD} through a pull-up resistor of 4.7 kΩ. The MODA pin also functions as the load instruction register ($\overline{LIR}$) pin when the MCU is not in reset. The $\overline{LIR}$ signal is useful during program debugging. The open-drain active low $\overline{LIR}$ output pin drives low during the first E cycle of each instruction. The MODB pin also functions as standby power input (V_{STBY}), which allows RAM contents to be maintained in absence of V_{DD}.

HPRIO — Highest Priority I-bit Interrupt and Miscellaneous **$103C**

	BIT 7	6	5	4	3	2	1	BIT 0
	RBOOT*	SMOD*	MDA*	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0
RESET:	0	0	0	0	0	0	0	0

*The reset values of RBOOT, SMOD, and MDA depend on the mode selected at power up.

RBOOT — Read Bootstrap ROM/EPROM

Valid only when SMOD is set (bootstrap or special test mode). Can only be written in special modes.

0 = Bootstrap ROM disabled and not in map

1 = Bootstrap ROM enabled and in map at $BF00–$BFFF

SMOD and MDA — Special Mode Select and Mode Select A

These two bits can be read at any time. They can be written anytime in special modes. MDA can only be written once in normal modes. SMOD cannot be set once it has been cleared.

Table 2 Operating Mode Selection

Inputs		Mode	Latched at Reset	
MODA	MODB		MDA	SMOD
0	1	Single Chip	0	0
1	1	Expanded	1	0
0	0	Bootstrap	0	1
1	0	Special Test	1	1

IRV(NE) — Internal Read Visibility(Not E)

IRVNE can be written once in any mode. In expanded modes, IRVNE determines whether IRV is on or off. In special test mode, IRVNE is reset to one. In all other modes, IRVNE is reset to zero.

0 = No internal read visibility on external bus

1 = Data from internal reads is driven out the external data bus.

In single-chip modes this bit determines whether the E clock drives out from the chip.

0 = E is driven out from the chip.

1 = E pin is driven low. Refer to the following table.

Table 3 IRVNE Control vs. Operating Mode

Operating Mode	IRVNE Bit Out of Reset	E Clock Out of Reset	IRV Function Out of Reset	IRVNE Bit Affects Only
Single Chip	0	On	Off	E
Expanded	0	On	Off	IRV
Bootstrap	0	On	Off	E
Special Test	1	On	On	IRV

PSEL[3:0] — Priority Select Bits [3:0]

Refer to **5 Resets and Interrupts**

4.6 RAM

In all modes RAM is enabled and present at locations $0000–$01FF. The RAM can be mapped to any 1-Kbyte boundary by writing an appropriate value to the INIT register. The INIT register must be written during the first 64 cycles after reset in expanded and single-chip modes. If RAM and the register block are placed at the same 1-Kbyte boundary, the first 64 bytes of RAM are inaccessible. This is due to an on-chip hardware priority scheme which eliminates conflicts which could arise from multiple resources sharing address locations. **Figure 6** shows the location of the RAM array.

4.7 Bootstrap ROM

When operating in normal modes (SMOD = 0), the bootstrap ROM is disabled and removed from the memory map. In bootstrap and special test modes, bootstrap ROM is present at $BF00–$BFFF. Bootstrap ROM cannot be remapped to other locations. **Figure 6** shows the location of the bootstrap ROM array.

The bootstrap ROM contains a small program that allows program code to be downloaded into on-chip RAM. When the MC68HC(7)11EA9 enters bootstrap mode, bootloader firmware residing in bootstrap ROM begins the downloading procedure by initializing the SCI system and transmitting a break out the SCI TxD pin. The SCI then waits for the first character to be received. After the first character is received on the RxD pin of the SCI, bootloader firmware begins counting the number of bytes received. When an idle time of four characters or the character for address $01FF is received, the bootloader program terminates the download and control is passed to the loaded program at $0000. For a detailed description of the M68HC11 bootstrap mode, refer to application note *M68HC11 Bootstrap Mode* (AN1060/D).

4.8 Memory Map and Register Block

The operating mode determines memory mapping and whether external addresses can be accessed. Memory locations for on-chip resources are the same for both expanded and single-chip modes. Control bits in the CONFIG register allow ROM/EPROM and EEPROM to be disabled from the memory map. The RAM is mapped to $0000 after reset. It can be placed at any 4 Kbyte boundary ($x000) by writing an appropriate value to the INIT register. The 64-byte register block is mapped to $1000 after reset and can also be placed at any 4 Kbyte boundary ($x000) by writing an appropriate value to the INIT register. If RAM and registers are mapped to the same boundary, the first 64 bytes of RAM will be inaccessible. **Table 4** shows the arrangement of control registers and bits within the register block.

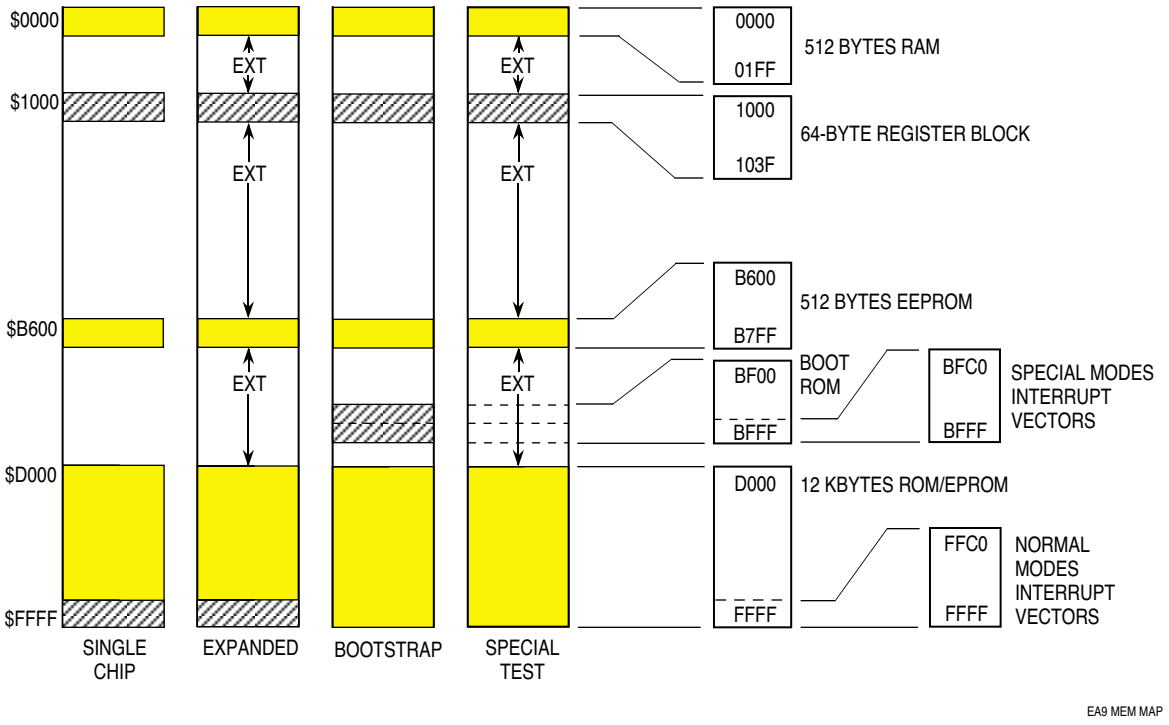


Figure 6 MC68HC(7)11EA9 Memory Map

INIT — RAM and I/O Mapping Register **$103D**

	BIT 7	6	5	4	3	2	1	BIT 0
	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
RESET:	0	0	0	0	0	0	0	1

RAM[3:0] — RAM Map Position

These four bits, which specify the upper hexadecimal digit of the RAM address, control position of RAM in the memory map. RAM can be positioned at the beginning of any 4 Kbyte page in the memory map. It is initialized to address $0000 out of reset.

REG[3:0] — 64-Byte Register Block Position

These four bits specify the upper hexadecimal digit of the address for the 64-byte block of internal registers. The register block, positioned at the beginning of any 4 Kbyte page in the memory map, is initialized to address $1000 out of reset.

Table 4 MC68HC(7)11EA9 Registers (Sheet 1 of 2)

	BIT 7	6	5	4	3	2	1	BIT 0	
$1000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$1001	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC
$1003	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$1004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$1005	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0	PORTCL
$1006	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
$1007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
$1008	XPIN	IPIN	0	0	0	0	PD1	PD0	PORTD
$1009	DISX	DISI	0	0	0	0	DDD1	DDD0	DDRD
$100A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
$100E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (HI)
$100F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (LO)
$1010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (HI)
$1011	Bit 7	6	5	4	3	2	1	Bit 0	TIC1 (LO)
$1012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (HI)
$1013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (LO)
$1014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (HI)
$1015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (LO)
$1016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1 (HI)
$1017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (LO)
$1018	Bit 15	14	13	12	11	10	9	Bit 8	TOC2 (HI)
$1019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (LO)
$101A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (HI)
$101B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (LO)
$101C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (HI)
$101D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (LO)
$101E	Bit 15	14	13	12	11	10	9	Bit 8	TI4/O5 (HI)
$101F	Bit 7	6	5	4	3	2	1	Bit 0	TI4/O5 (LO)
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
$1022	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I	TMSK1
$1023	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F	TFLG1
$1024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
$1025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2
$1026	0	PAEN	PAMOD	PEDGE	0	I4/O5	RTR1	RTR0	PACTL
$1027	Bit 7	6	5	4	3	2	1	Bit 0	PACNT
$1028	BTST	BSPL	BRST	SBR12	SBR11	SBR10	SBR9	SBR8	SCBDH
$1029	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	SCBDL
$102A	LOOPS	WOMS	0	M	WAKE	ILT	PE	PT	SCCR1
$102B	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
$102C	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF	SCSR1
$102D	0	0	0	0	0	0	0	RAF	SCSR2
$102E	R8	T8	0	0	0	0	0	0	SCDRH

Table 4 MC68HC(7)11EA9 Registers (Sheet 2 of 2)

	BIT 7	6	5	4	3	2	1	BIT 0	
$102F	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SCDRL
$1030	CCF	0	SCAN	MULT	CD	CC	CB	CA	ADCTL
$1031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$1032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$1033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$1034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4
$1035	0	0	0	PTCON	BPRT3	BPRT2	BPRT1	BPRT0	BPROT
$1036	PLLON	BCS	AUTO	BWC	VCOT	MCS	LCK	WEN	PLLCR
$1037	SYNX1	SYNX0	SYNY5	SYNY4	SYNY3	SYNY2	SYNY1	SYNY0	SYNR
$1038									Reserved
$1039	ADPU	CSEL	IRQE	DLY	CME	0	CR1	CR0	OPTION
$103A	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
$103B	ODD	EVEN	ELAT[1]	BYTE	ROW	ERASE	EELAT	PGM	PPROG
$103C	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
$103E	—	—	—	—	—	—	—	—	TEST1[2]
$103F	0	0	0	0	NOSEC	NOCOP	ROMON	EEON	CONFIG

Notes:
1. MC68HC711EA9 only.
2. Factory test only.

4.9 ROM/EPROM/OTPROM

The MC68HC11EA9 contains 12 Kbytes of mask-programmed ROM. The ROM array is programmed at the factory to customer specifications and cannot be altered. The ROM array can be disabled by clearing the ROMON bit in the CONFIG register.

The MC68HC711EA9 MCU contains 12 Kbytes of on-chip EPROM/OTPROM. When the MC68HC711EA9 is packaged in a windowed CLCC, the 12 Kbytes of EPROM may be erased by exposing the device to ultraviolet light. An MC68HC711EA9 MCU packaged in a non-windowed case contains 12 Kbytes of one-time-programmable ROM (OTPROM).

Using the on-chip EPROM/OTPROM programming feature requires an external 12.25-volt power supply (V_{PPE}). Normal programming is accomplished using the EPROM/OTPROM programming register (PPROG). PPROG is the combined EPROM/OTPROM and EEPROM programming register (MC68HC711EA9 only). For the MC68HC11EA9, PPROG is used for programming EEPROM only. There are three possible methods of programming and verifying EPROM.

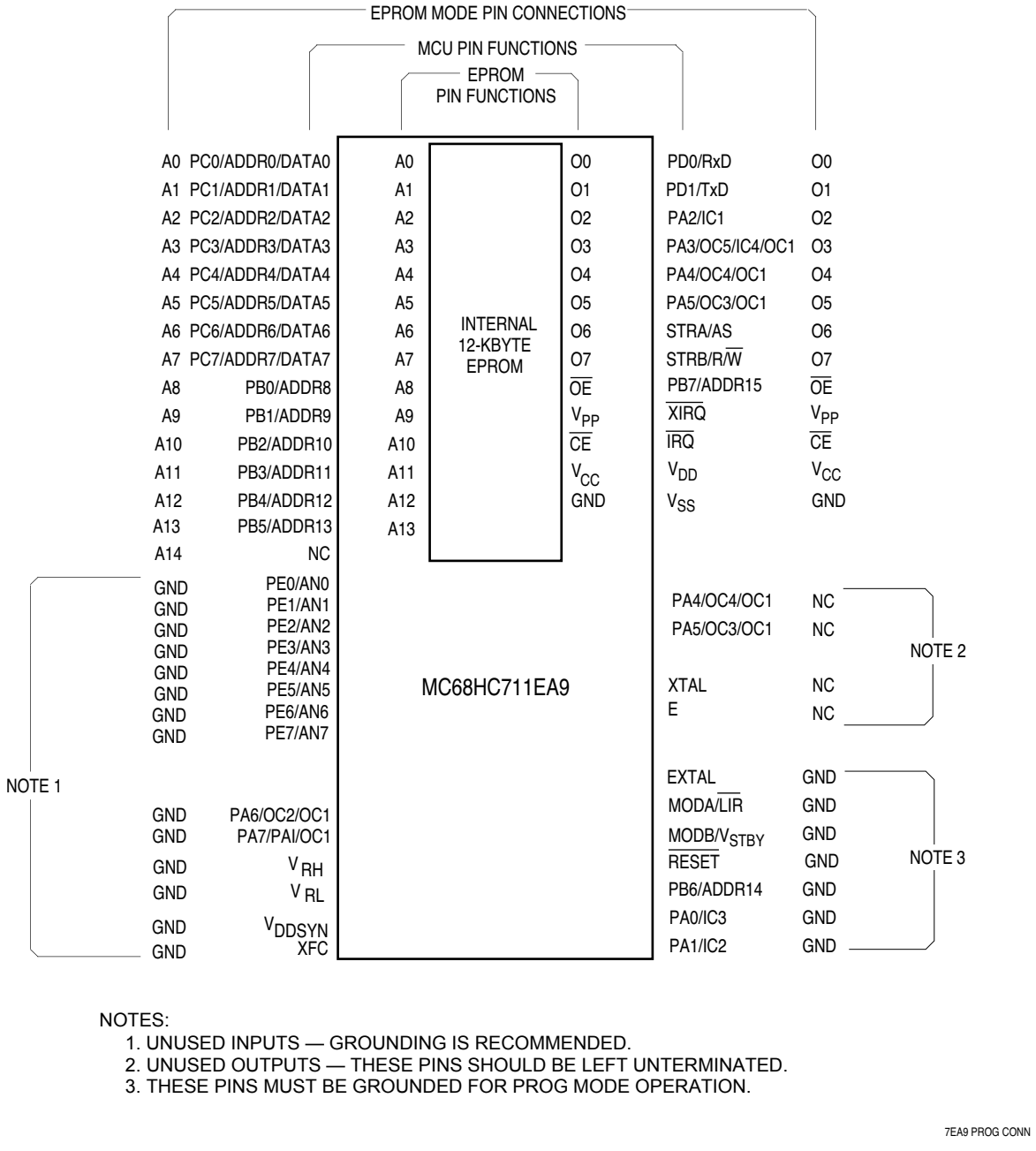
4.9.1 EPROM Emulation Mode

The EPROM emulation (PROG) mode allows the on-chip EPROM/OTPROM to be programmed as a standard EPROM by adapting the MCU footprint to that of the 27256-type EPROM, as shown in **Figure 7**. Grounding the $\overline{\text{RESET}}$, MODA, and MODB pins places the MCU in PROG mode. An appropriate EPROM programmer can then be used to enter data into the on-chip EPROM. **Figure 7** shows the MCU pin functions while the device is in PROG mode.

If the MCU is operating with programming voltage present on the $\overline{\text{XIRQ}}/V_{PPE}$ pin, the $\overline{\text{IRQ}}$ pin ($\overline{\text{CE}}$ pin in PROG mode) must be pulled high before the address and data are changed to program the next location.

NOTE

PROG mode is disabled in devices having the security feature.



NOTES:
1. UNUSED INPUTS — GROUNDING IS RECOMMENDED.
2. UNUSED OUTPUTS — THESE PINS SHOULD BE LEFT UNTERMINATED.
3. THESE PINS MUST BE GROUNDED FOR PROG MODE OPERATION.

7EA9 PROG CONN

Figure 7 MC68HC711EA9 PROG Mode Connections

4.9.2 Programming an Individual EPROM Address

In the second method, the MCU programs its own EPROM by controlling the PPROG register. Use the following procedure to program the EPROM through the MCU with the ROMON bit set in the CONFIG register. The 12 volt nominal programming voltage must be present on the $\overline{XIRQ}/V_{PPE}$ pin. Any operating mode can be used.

1. Write to PPROG to set the ELAT bit.
2. Write the data to the desired address.
3. Write to PPROG to set both the ELAT and PGM bits.
4. Delay for 10 ms or more, as appropriate.

5. Clear the PGM bit to turn off the V_{PPE} voltage.
6. Clear all bits in the PPROG register to reconfigure the EPROM address and data buses for normal operation.

NOTE

PROG mode is initiated when $\overline{\text{RESET}}$, $\overline{\text{MODA}}$, and $\overline{\text{MODB}}$ pins are pulled low (the pin state required to enter bootstrap mode). This means that if these three pins are pulled low and V_{PPE} is present on the $\overline{\text{XIRQ}}$ pin, the EPROM will be programmed. To prevent this, place a pull-up resistor on the $\overline{\text{IRQ}}$ pin ($\overline{\text{CE}}$ pin in PROG mode). When the device goes into reset, the PGM bit is forced to the voltage disable state (EPGM = 0) before the address/data latches are enabled to the external input lines. Only after this occurs is voltage control returned to the $\overline{\text{IRQ}}$ pin.

4.9.3 Programming EPROM with Downloaded Data

When using this method, the EPROM is programmed by software while in the special test or bootstrap modes. User-developed software can be uploaded through the SCI, or a ROM resident EPROM programming utility can be used. To use the resident utility, bootload a three-byte program consisting of a single jump instruction to $BF00. $BF00 is the starting address of a resident EPROM programming utility. The utility program sets the X and Y index registers to default values, then receives programming data from an external host and puts it in EPROM. The value in IX determines programming delay time. The value in IY is a pointer to the first address in EPROM to be programmed (default = $D000).

When the utility program is ready to receive programming data, it sends the host the $FF character. Then it waits. When the host sees the $FF character, the EPROM programming data is sent, starting with the first location in the EPROM array. After the last byte to be programmed is sent and the corresponding verification data is returned, the programming operation is terminated by resetting the MCU.

PPROG — EPROM and EEPROM Programming Control Register **$103B**

	BIT 7	6	5	4	3	2	1	BIT 0
	ODD	EVEN	ELAT*	BYTE	ROW	ERASE	EELAT	PGM
RESET:	0	0	0	0	0	0	0	1

* MC68HC711EA9 only.

ODD — Program Odd Rows in Half of EEPROM (TEST)
Refer to **4.10 EEPROM**.

EVEN — Program Even Rows in Half of EEPROM (TEST)
Refer to **4.10 EEPROM**.

ELAT — EPROM/OTPROM Latch Control
When ELAT = 1, writes to EPROM cause address and data to be latched and the EPROM/OTPROM cannot be read. ELAT can be read any time. ELAT can be written any time except when EPGM = 1; then the write to ELAT is disabled. For MC68HC711EA9, EPGM enables the high voltage necessary for both EPROM/OTPROM and EEPROM programming. For MC68HC711EA9 ELAT and EELAT are mutually exclusive and cannot both equal one.
0 = EPROM address and data bus configured for normal reads
1 = EPROM address and data bus configured for programming

BYTE — Byte/Other EEPROM Erase Mode
Refer to **4.10 EEPROM**.

ROW — Row/All EEPROM Erase Mode
Refer to **4.10 EEPROM**.

ERASE — Erase/Normal Control for EEPROM
Refer to **4.10 EEPROM**.

EELAT — EEPROM Latch Control
0 = EEPROM address and data bus configured for normal reads
1 = EEPROM address and data bus configured for programming or erasing

PGM — EPROM/OTPROM/EEPROM Programming Voltage Enable
0 = Programming voltage to EPROM/OTPROM/EEPROM array disconnected
1 = Programming voltage to EPROM/OTPROM/EEPROM array connected
PGM can be read any time and can only be written when ELAT = 1 (for EPROM/OTPROM programming) or when EELAT = 1 (for EEPROM programming).

4.10 EEPROM

MC68HC(7)11EA9 MCUs contain 512 bytes of EEPROM. The 512-byte EEPROM is initially located at $B600 after reset, assuming EEPROM is enabled in the memory map by the EEON bit in the CONFIG register. EEPROM can be placed at any 4 Kbyte boundary ($x600) by writing appropriate values to the INIT register. Note that EEPROM can be mapped such that it contains the vector space. See **Figure 6**.

4.10.1 Programming and Erasing EEPROM

Programming and erasing the EEPROM is controlled by the PPROG register, and is dependent upon the block protect (BPROT) register value. The erased state of an EEPROM bit is one. During a read operation, bit lines are precharged to one. The floating gate devices of programmed bits conduct and pull the bit lines to zero. Unprogrammed bits remain at the precharged level and are read as ones. Programming a bit to one causes no change. Programming a bit to zero changes the bit so that subsequent reads return zero.

When appropriate bits in the BPROT register are cleared, the PPROG register controls programming and erasing of the EEPROM. The PPROG register can be read or written at any time, but logic enforces defined programming and erasing sequences to prevent unintentional changes to data in EEPROM. When the EELAT bit in the PPROG register is cleared, the EEPROM can be read as if it were a ROM.

The on-chip charge pump that generates the EEPROM programming voltage from V_{DD} uses MOS capacitors, which are relatively small in value. The efficiency of this charge pump and its drive capability are affected by the level of V_{DD} and the frequency of the driving clock. The clock source driving the charge pump is software selectable. When the clock select (CSEL) bit in the OPTION register is zero, the E clock is used; when CSEL is one, an on-chip resistor-capacitor (RC) oscillator is used. The RC oscillator should be used when E < 1 MHz. This RC oscillator will drive the A/D circuitry as well as the EEPROM charge pump when CSEL = 1.

The EEPROM programming voltage connection to the EEPROM array is not enabled until there has been a write to PPROG with EELAT set and PGM cleared. This must be followed by a write to a valid EEPROM location or to the CONFIG address, and then a write to PPROG with both EELAT and PGM set. Any attempt to set both EELAT and PGM during the same write operation results in neither bit being set.

The erased state of an EEPROM byte is $FF (all ones).

To erase the EEPROM, ensure that the proper bits of the BPROT register are cleared, then complete the following steps using the PPROG register:

1. Set the ERASE, EELAT, and appropriate BYTE and ROW bits in PPROG register.
2. Write to the appropriate EEPROM address with any data. Row erase only requires a write to any location in the row. Bulk erase is done by writing to any location in the array.
3. Set the ERASE, EELAT, EEPGM, and appropriate BYTE and ROW bits in PPROG register.

4. Delay for 10 ms or more, as appropriate.
5. Clear the EEPGM bit in PPROG to turn off the programming voltage.
6. Clear the PPROG register to reconfigure the EEPROM address and data buses for normal operation.

To program the EEPROM, ensure the proper bits of the BPROT register are cleared and use the PROG register to complete the following steps:

1. Set the EELAT bit in PPROG register.
2. Write data to the desired address.
3. Set EEPGM bit in PPROG.
4. Delay for 10 ms or more, as appropriate.
5. Clear the EEPGM bit in PPROG to turn off the programming voltage.
6. Clear the PPROG register to reconfigure the EEPROM address and data buses for normal operation.

CAUTION

Since it is possible to perform other operations while the EEPROM programming/erase operation is in progress, it is common to start the operation then return to the main program until the 10 ms is completed. When the EELAT bit is set at the beginning of a program/erase operation, the EEPROM is electronically removed from the memory map; thus, it is not accessible during the program/erase cycle. Care must be taken to ensure that EEPROM resources will not be needed by any routines in the code during the 10 ms program/erase time.

BPROT — EEPROM Block Protect **$1035**

	BIT 7	6	5	4	3	2	1	BIT 0
	—	—	—	PTCON	BPRT3	BPRT2	BPRT1	BPRT0
RESET:	0	0	0	1	1	1	1	1

Active bits in BPROT reset to ones in all modes and can only be cleared during the first 64 cycles out of reset. Bits can be set only once in normal modes. In special modes, bits can be set and cleared repeatedly.

Bits [7:5] — Not implemented
Always read zero

PTCON — Protect CONFIG Register
0 = CONFIG register can be programmed or erased normally
1 = CONFIG register cannot be programmed or erased

BPRT[3:0] — Block Protect Bits for EEPROM
When set, these bits protect a block of EEPROM from being programmed or electronically erased. Ultraviolet light, however can erase the entire EEPROM contents regardless of BPRT[3:0] (windowed packages only). When cleared, they allow programming and erasure of the associated block.

Table 5 EEPROM Block Protect

Bit Name	Block Protected	Block Size
BPRT0	$B600–$B61F	32 Bytes
BPRT1	$B620–$B65F	64 Bytes
BPRT2	$B660–$B6DF	128 Bytes
BPRT3	$B6E0–$B7FF	288 Bytes

PPROG — EPROM and EEPROM Programming Control Register **$103B**

	BIT 7	6	5	4	3	2	1	BIT 0
	ODD	EVEN	ELAT*	BYTE	ROW	ERASE	EELAT	PGM
RESET:	0	0	0	0	0	0	0	1

* MC68HC711EA9 only.

ODD — Program Odd Rows in Half of EEPROM (TEST)

EVEN — Program Even Rows in Half of EEPROM (TEST)

ELAT — EPROM/OTPROM Latch Control
MC68HC711EA9 only. Refer to **4.9.3 Programming EPROM with Downloaded Data**.

BYTE — Byte/Other EEPROM Erase Mode
0 = Row or bulk erase mode used
1 = Erase only one byte of EEPROM

ROW — Row/All EEPROM Erase Mode (only valid when BYTE = 0)
0 = All 512 bytes of EEPROM erased
1 = Erase only one 16-byte row of EEPROM

Table 6 BYTE/ROW Control Bits

BYTE	ROW	Action
0	0	Bulk Erase (All 512 Bytes)
0	1	Row Erase (16 Bytes)
1	0	Byte Erase
1	1	Byte Erase

ERASE — Erase/Normal Control for EEPROM
0 = Normal read or program mode
1 = Erase mode

EELAT — EEPROM Latch Control
0 = EEPROM address and data bus configured for normal reads
1 = EEPROM address and data bus configured for programming or erasing

PGM — EPROM/OTPROM/EEPROM Programming Voltage Enable
0 = Programming voltage to EPROM/OTPROM/EEPROM array disconnected
1 = Programming voltage to EPROM/OTPROM/EEPROM array connected
PGM can be read any time and can only be written when ELAT = 1 (for EPROM/OTPROM programming) or when EELAT = 1 (for EEPROM programming).

4.10.2 CONFIG Register

The CONFIG register consists of an EEPROM byte and static latches that control the start-up configuration of the MCU. The contents of the EEPROM byte are transferred into static working latches during reset sequences. The operation of the MCU is controlled directly by these latches and not by CONFIG itself. Although the byte is not included in the 512-byte EEPROM array, programming the CONFIG register requires the same procedure as any byte in the array. In normal modes, changes to CONFIG do not affect operation of the MCU until after the next reset sequence. When programming, the CONFIG register itself is accessed. When the CONFIG register is read, the static latches are accessed.

CONFIG — Security, COP, ROM/EPROM, and EEPROM Enables **$103F**

	BIT 7	6	5	4	3	2	1	BIT 0
	—	—	—	—	NOSEC	NOCOP	ROMON	EEON
RESETS:								
S. Chip:	0	0	0	0	U	U	1	U
Boot:	0	0	0	0	U	U(L)	U	U
Exp.:	0	0	0	0	1	U	U	U
Test:	0	0	0	0	1	U(L)	U	U

U indicates a previously programmed bit. U(L) indicates that the bit resets to the logic level held in the latch prior to reset (unchanged), but the function of COP is controlled by DISR bit in TEST1 register.

Bits [7:4] — Not Implemented
Always read zero

NOSEC — Security Disable
NOSEC is invalid unless the security mask option is specified before the MCU is manufactured. If security mask option is omitted NOSEC always reads one. The security feature protects the contents of RAM and EEPROM.
0 = Security enabled
1 = Security disabled

NOCOP — COP System Disable
Refer to **5 Resets and Interrupts**.

ROMON — ROM/EPROM/OTPROM Enable
When this bit is zero, the ROM or EPROM/OTPROM is disabled and that memory space becomes externally addressed. In single-chip mode, ROMON is forced to one to enable ROM/EPROM/OTPROM regardless of the state of the ROMON bit.
0 = ROM/EPROM/OTPROM disabled from the memory map
1 = ROM/EPROM/OTPROM present in the memory map

EEON — EEPROM Enable
When this bit is zero, the EEPROM is disabled and that memory space becomes externally addressed.
0 = EEPROM removed from the memory map
1 = EEPROM present in the memory map

4.10.3 EEPROM Security

The optional security feature, available only on ROM-based MCUs, protects the EEPROM and RAM contents from unauthorized access. A program, or a key portion of a program, can be protected against unauthorized duplication. To accomplish this, the protection mechanism restricts operation of protected devices to the single-chip modes. This prevents the memory locations from being monitored externally because single-chip modes do not allow visibility of the internal address and data buses. Resident programs, however, have unlimited access to the internal EEPROM and RAM and can read, write, or transfer the contents of these memories.

5 Resets and Interrupts

All M68HC11 MCUs have three reset vectors and 18 interrupt vectors. The reset vectors are as follows:

- $\overline{\text{RESET}}$, or Power-On Reset
- Clock Monitor Fail
- COP Failure

The 18 interrupt vectors service 22 interrupt sources (3 non-maskable, 19 maskable). The 3 non-maskable interrupt sources are as follows:

- Illegal Opcode Trap
- Software Interrupt
- $\overline{\text{XIRQ}}$ Pin (X Interrupt)

On-chip peripheral systems generate maskable interrupts, which are recognized only if the global interrupt mask bit (I) in the condition code register (CCR) is clear. Maskable interrupts are prioritized according to a default arrangement; however, any one source can be elevated to the highest maskable priority position by a software-accessible control register (HPRIO). The HPRIO register can be written at any time, provided bit I in the CCR is set.

Eighteen interrupt sources in the MC68HC(7)11EA9 MCUs are subject to masking by the global interrupt mask bit (bit I in the CCR). In addition to the global bit I, all of these sources, except the external interrupt ($\overline{\text{IRQ}}$) pin, are controlled by local enable bits in control registers. Most interrupt sources in the M68HC11 have separate interrupt vectors; therefore, there is usually no need for software to poll control registers to determine the cause of an interrupt.

For some interrupt sources, such as the SCI interrupts, the flags are automatically cleared during the normal course of responding to the interrupt requests. For example, the RDRF flag in the SCI system is cleared by the automatic clearing mechanism invoked by a read of the SCI status register while RDRF is set, followed by a read of the SCI data register. The normal response to an RDRF interrupt request would be to read the SCI status register to check for receive errors, then to read the received data from the SCI data register. These two steps satisfy the automatic clearing mechanism without requiring any special instructions.

The computer operating properly (COP) watchdog and the clock monitor are both circuits that force a reset sequence when a malfunctioning clock is encountered. The COP function forces a reset when a timeout occurs. The timeout period is determined by programming CR[1:0] in OPTION register. The clock monitor circuit forces a reset sequence whenever the clock is slow or absent. The CME bit in the OPTION register enables the clock monitor circuit. To use STOP mode the clock monitor must be disabled before the STOP instruction is executed or a reset sequence will occur.

Refer to the following table for a list of interrupt and reset vector assignments.

Table 7 Interrupt and Reset Vector Assignments

Vector Address	Interrupt Source	CCR Mask	Local Mask	Priority (1 = High)
FFC0, C1 — FFD4, D5	Reserved	—	—	—
FFD6, D7	SCI Serial System	Bit I		18
	• SCI Receive Data Register Full		RIE	
	• SCI Receiver Overrun		RIE	
	• SCI Transmit Data Register Empty		TIE	
	• SCI Transmit Complete		TCIE	
	• SCI Idle Line Detect		ILIE	
FFD8, D9	Reserved	—	—	—

Table 7 Interrupt and Reset Vector Assignments

FFDA, DB	Pulse Accumulator Input Edge	Bit I	PAII	17
FFDC, DD	Pulse Accumulator Overflow	Bit I	PAOVI	16
FFDE, DF	Timer Overflow	Bit I	TOI	15
FFE0, E1	Timer Input Capture 4/Output Compare 5	Bit I	I4/O5I	14
FFE2, E3	Timer Output Compare 4	Bit I	OC4I	13
FFE4, E5	Timer Output Compare 3	Bit I	OC3I	12
FFE6, E7	Timer Output Compare 2	Bit I	OC2I	11
FFE8, E9	Timer Output Compare 1	Bit I	OC1I	10
FFEA, EB	Timer Input Capture 3	Bit I	IC3I	9
FFEC, ED	Timer Input Capture 2	Bit I	IC2I	8
FFEE, EF	Timer Input Capture 1	Bit I	IC1I	7
FFF0, F1	Real-Time Interrupt	Bit I	RTII	6
FFF2, F3	$\overline{\text{IRQ}}$ (External Pin)	Bit I	None	5
FFF4, F5	$\overline{\text{XIRQ}}$ Pin	Bit X	None	4
FFF6, F7	Software Interrupt	None	None	*
FFF8, F9	Illegal Opcode Trap	None	None	*
FFFA, FB	COP Failure	None	NOCOP	3
FFFC, FD	Clock Monitor Fail	None	CME	2
FFFE, FF	RESET	None	None	1

* Same level as an instruction

OPTION — System Configuration Options **$1039**

	BIT 7	6	5	4	3	2	1	BIT 0
	ADPU	CSEL	IRQE*	DLY*	CME	—	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

* Can be written only once in first 64 cycles after reset in normal modes, or at any time in special modes.

ADPU — A/D Converter Power up
Refer to **9 Analog-to-Digital Converter**

CSEL — Clock Select
Refer to **4.10 EEPROM**.

IRQE — $\overline{\text{IRQ}}$ Select Edge-Sensitive Only
0 = $\overline{\text{IRQ}}$ input is active-low
1 = $\overline{\text{IRQ}}$ input recognizes falling edges only

DLY — Enable Oscillator Start-up Delay
0 = No stabilization delay on exit from STOP mode.
1 = A delay of approximately 4000 E-clock cycles is imposed as the MCU exits STOP mode.

CME — Clock Monitor Enable
0 = Clock monitor disabled; slow clock can be used.
1 = Slow or stopped clocks cause COP failure reset.

Bit 2 — Not implemented
Always reads zero

CR[1:0] — COP Timer Rate Select
Refer to the following table of COP timer rates.

Table 8 COP Timer Rate Selection

CR[1:0]	Rate Selected	Period Length		
		E = 1.0 MHz	E = 2.0 MHz	E = 3.0 MHz
0 0	$2^{15} \div E$	32.768 ms	16.384 ms	10.923 ms
0 1	$2^{17} \div E$	131.072 ms	65.536 ms	43.691 ms
1 0	$2^{19} \div E$	524.288 ms	262.140 ms	174.76 ms
1 1	$2^{21} \div E$	2.097 s	1.049 s	699.05 ms

COPRST — Arm/Reset COP Timer Circuitry **$103A**

	BIT 7	6	5	4	3	2	1	BIT 0
	7	6	5	4	3	2	1	0
RESET:	0	0	0	1	0	0	0	0

Write $55 to COPRST to arm COP watchdog circuit. Write $AA to COPRST to reset COP watchdog circuit.

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous **$103C**

	BIT 7	6	5	4	3	2	1	BIT 0
	RBOOT*	SMOD*	MDA*	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0
RESET:	—	—	—	0	0	1	0	1

*RBOOT, SMOD, and MDA reset depend on power-up initialization mode and can only be written in special mode.

RBOOT — Read Bootstrap ROM
Refer to **4.4 Bootstrap Mode**

SMOD — Special Mode Select
Refer to **4.5 Mode Selection**

MDA — Mode Select A
Refer to **4.5 Mode Selection**

IRVNE — Internal Read Visibility/Not E
Refer to **4.5 Mode Selection**

PSEL[3:0] — Priority Select Bit 4 through Bit 0
Can be written only while the I-bit in the CCR is set (interrupts disabled). These bits select one interrupt source to be elevated above all other I-bit related sources.

Table 9 Highest I-Bit Interrupt Source Selection

PSEL3	PSEL2	PSEL1	PSEL0	Interrupt Source Promoted
0	0	0	0	Timer Overflow
0	0	0	1	Pulse Accumulator Overflow
0	0	1	0	Pulse Accumulator Input Edge
0	0	1	1	Reserved (Default to $\overline{\text{IRQ}}$)
0	1	0	0	SCI Serial System
0	1	0	1	Reserved (Default to $\overline{\text{IRQ}}$)
0	1	1	0	IRQ (External Pin)
0	1	1	1	Real-Time Interrupt
1	0	0	0	Timer Input Capture 1
1	0	0	1	Timer Input Capture 2
1	0	1	0	Timer Input Capture 3
1	0	1	1	Timer Output Compare 1
1	1	0	0	Timer Output Compare 2
1	1	0	1	Timer Output Compare 3
1	1	1	0	Timer Output Compare 4
1	1	1	1	Timer IC4/OC5

PSEL[3:0] reset to %0101, making $\overline{\text{IRQ}}$ the highest priority I-bit related interrupt source.

CONFIG — Security, COP, ROM/EPROM, and EEPROM Enables **$103F**

	BIT 7	6	5	4	3	2	1	BIT 0
	—	—	—	—	NOSEC	NOCOP	ROMON	EEON
RESET:	—	—	—	0	0	1	0	1

Bits [7:4] — Not Implemented
Always read zero

NOSEC — EEPROM Security Mode Disable
Refer to **4.10.3 EEPROM Security**

NOCOP — COP System Disable
0 = COP system enabled (forces reset on timeout)
1 = COP system disabled

ROMON — ROM/EPROM Enable
Refer to **4 Operating Modes and On-Chip Memory**.

EEON — EEPROM Enable
Refer to **4.10 EEPROM**

6 Parallel Input/Output

The MC68HC(7)11EA9 has up to 36 input/output lines, depending on the operating mode. **Table 10** shows the configuration and features of each port.

Table 10 I/O Port Configuration

Port	Input Pins	Output Pins	Bidirectional Pins	Shared Functions
A	—	—	8	Timer
B	—	—	8	High Order Address
C	—	—	8	Multiplexed Low Order Address/Data
D	—	—	2	SCI/PLL Test
E	8	—	—	A/D Converter
—	1	—	—	XPIN ($\overline{\text{XIRQ}}$ pin configured for data input)
—	1	—	—	IPIN ($\overline{\text{IRQ}}$ pin configured for data input)

Simple and full handshake input and output functions are available on ports B and C lines in single-chip mode. The following is a description of the handshake functions.

In simple strobed mode, port B is a strobed output port and port C is a latching input port. The two activities are available simultaneously.

The STRB output is pulsed for two E-clock periods each time there is a write to the PORTB register. The INVB bit in the PIOC register controls the polarity of STRB pulses. Port C levels are latched into the alternate port C latch (PORTCL) register on each assertion of the STRA input. STRA edge select, flag, and interrupt enable bits are located in the PIOC register. Any or all of the port C lines can still be used as general-purpose I/O while in strobed input mode.

Full handshake modes involve port C pins and the STRA and STRB lines. Input and output handshake modes are supported, and output handshake mode has a three-stated variation. STRA is an edge detecting input, and STRB is a handshake output. Control and enable bits are located in the PIOC register.

In full input handshake mode, the MCU uses STRB as a ready line to an external system. Port C logic levels are latched into PORTCL when the STRA line is asserted by the external system. The MCU then negates STRB. The MCU reasserts STRB after the PORTCL register is read. A mix of latched inputs, static inputs, and static outputs is allowed on port C, differentiated by the data direction bits and use of the PORTC and PORTCL registers.

In full output handshake mode, the MCU writes data to PORTCL which, in turn, asserts the STRB output to indicate that data is ready. The external system reads port C and asserts the STRA input to acknowledge that data has been received.

In the three-state variation of output handshake mode, lines intended as three-state handshake outputs are configured as inputs by clearing the corresponding DDRC bits. The MCU writes data to PORTCL and asserts STRB. The external system responds by activating the STRA input, which forces the MCU to drive the data in PORTCL out on all of the port C lines. The mode variation does not allow part of port C to be used for static inputs while other port C pins are being used for handshake outputs. Refer to PIOC register description for further information.

PIOC — Port I/O Control **$1002**

	BIT 7	6	5	4	3	2	1	BIT 0
	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB
RESET:	0	0	0	0	0	0	0	0

STAF — Strobe A Interrupt Status Flag

This bit is set when a selected edge occurs on Strobe A. Clearing it depends on the state of the HNDS and OIN bits. In simple strobed mode or in full handshake mode, STAF is cleared by a read of the PIOC register followed by a read of PORTCL register. In output handshake mode, STAF is cleared by reading the PIOC register followed by a write to PORTCL register.

0 = No edge detected on strobe A
1 = The selected edge (rising or falling) has been detected on strobe A

STAI — Strobe A Interrupt Enable

When bit I in the condition code register is clear and STAI is set, STAF (when set) will request an interrupt.

0 = STAF will not generate an interrupt when set.
1 = STAF will generate an interrupt when set.

CWOM — Port C Wire-OR Mode

CWOM affects all eight port A pins.

0 = Port C outputs are normal CMOS outputs
1 = Port C outputs act as open-drain outputs

HNDS — Handshake Mode

When clear, strobe A acts as a simple input strobe to latch data into PORTCL, and strobe B acts as a simple output strobe which pulses after a write to port B. When set, a handshake protocol involving port C, STRA, and STRB is selected (see the definition for the OIN bit).

0 = Simple strobe mode
1 = Full input or output handshake mode

OIN — Output or Input Handshaking

This bit has no meaning or effect when HNDS = 0.

0 = Input handshake
1 = Output handshake

PLS — Pulse/Interlocked Handshake Operation

This bit has no meaning if HNDS = 0. When interlocked handshake operation is selected, strobe B, once activated, stays active until the selected edge of strobe A is detected. When pulsed handshake operation is selected, strobe B is pulsed for two E cycles.

0 = Interlocked handshake selected
1 = Pulsed handshake selected

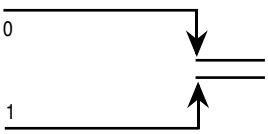
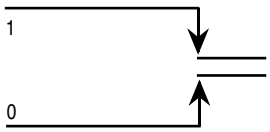
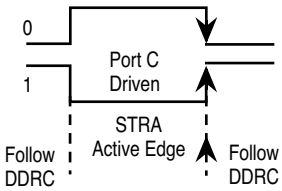
EGA — Active Edge for Strobe A

0 = Falling edge of strobe A selected. When output handshake is selected, port C lines obey the data direction register while STRA is low, but port C is forced to output when STRA is high.
1 = Rising edge of strobe A selected. When output handshake is selected, port C lines obey the data direction register while STRA is high, but port C is forced to output when STRA is low.

INVB — Invert Strobe B

0 = Active level is logic zero
1 = Active level is logic one

Table 11 Strobed and Handshake Parallel I/O Control Bit Summary

	STAF Clearing Sequence	HNDS	OIN	PLS	EGA	Port B	Port C
Simple strobed mode	Read PIOC with STAF = 1 then read PORTCL	0	X	X		Inputs latched into PORTCL on any active edge on STRA	STRB pulses on writes to PORTB
Full input handshake mode	Read PIOC with STAF = 1 then read PORTCL	1	0	0 = STRB active level 1 = STRB active pulse		Inputs latched into PORTCL on any active edge on STRA	Normal output port, unaffected in handshake modes
Full output handshake mode	Read PIOC with STAF = 1 then write PORTCL	1	1	0 = STRB active level 1 = STRB active pulse		Driven as outputs if STRA at active level; follows DDRC if STRA not at active level	Normal output port, unaffected in handshake modes

Port pin function is mode dependent. Do not confuse pin function with the electrical state of the pin at reset. Port pins are either driven to a specified logic level or are configured as high impedance inputs. I/O pins configured as high-impedance inputs have port data that is indeterminate. The contents of the corresponding latches are dependent upon the electrical state of the pins during reset. In port descriptions, an "I" indicates this condition. Port pins that are driven to a known logic level during reset are shown with a value of either one or zero. Some control bits are unaffected by reset. Reset states for these bits are indicated with a "U".

PORTA — Port A Data **$1000**

	BIT 7	6	5	4	3	2	1	BIT 0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	I	I	I	I	I	I	I	I
Alt. Pin Func.:	PAI	OC2	OC3	OC4	IC4/OC5	IC1	IC2	IC3
And/or	OC1	OC1	OC1	OC1	OC1	—	—	—

NOTE

The timer forces the I/O state to output for each port A line associated with an enabled output compare. In these cases the data direction bits will not be changed, but have no effect on these lines. The DDRA will revert to controlling data direction when the associated timer compare is disabled. Input captures do not force either the I/O state of the pin or the state of DDRA. To enable PA3 as fourth input capture, set the I4/O5 bit in the PACTL register. Otherwise, PA3 is configured as a fifth output compare out of reset, with bit I4/O5 being cleared. If the DDA3 bit in DDRA is set (configuring PA3 as an output), and IC4 is enabled, writes to PA3 cause edges on the pin to result in input captures. Writing to TI4/O5 has no effect when the TI4/O5 register is acting as IC4. PA7 drives the pulse accumulator input but also can be configured for general-purpose I/O or output compare. DDA7 bit in DDRA register configures PA7 for either input or output. Note that even when PA7 is configured as an output, the pin still drives the pulse accumulator input.

DDRA — Port A Data Direction **$1001**

	BIT 7	6	5	4	3	2	1	BIT 0
	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
RESET:	0	0	0	0	0	0	0	0

DDA[7:0] — Data Direction for Port A
0 = Corresponding pin configured for input
1 = Corresponding pin configured for output

PORTB — Port B Data **$1004**

	BIT 7	6	5	4	3	2	1	BIT 0
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	ADDR15	ADDR14	ADDR13	ADDR12	ADDR11	ADDR10	ADDR9	ADDR8

DDRB — Port B Data Direction **$1006**

	BIT 7	6	5	4	3	2	1	BIT 0
	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
RESET:	0	0	0	0	0	0	0	0

DDB[7:0] — Data Direction for Port B
0 = Corresponding pin configured for input
1 = Corresponding pin configured for output

PORTC — Port C Data **$1003**

	BIT 7	6	5	4	3	2	1	BIT 0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
Or:	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

PORTCL — Port C Latched Data **$1005**

	BIT 7	6	5	4	3	2	1	BIT 0
	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
RESET:	0	0	0	0	0	0	0	0

PORTCL is used in the handshake clearing mechanism. When an active edge occurs on the STRA pin, port C data is latched into the PORTCL register. Reads of this register return the last value latched into PORTCL and clear STAF flag (following a read of PIOC with STAF set).

DDRC — Port C Data Direction **$1007**

	BIT 7	6	5	4	3	2	1	BIT 0
	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
RESET:	0	0	0	0	0	0	0	0

DDC[7:0] — Data Direction for Port C
0 = Corresponding pin configured for input
1 = Corresponding pin configured for output

PORTD — Port D Data **$1008**

	BIT 7	6	5	4	3	2	1	BIT 0
	XPIN	IPIN	—	—	—	—	PD1	PD0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	—	—	—	—	—	—	TxD	RxD

XPIN — $\overline{\text{XIRQ}}$ Interrupt Pin Status Flag

This is a read-only bit. XPIN reflects the logic level present on the $\overline{\text{XIRQ}}$ pin.

0 = $\overline{\text{XIRQ}}$ pin low.
1 = $\overline{\text{XIRQ}}$ pin high.

IPIN — $\overline{\text{IRQ}}$ Interrupt Pin Status Flag

This is a read-only bit. IPIN reflects the logic level present on the $\overline{\text{IRQ}}$ pin.

0 = $\overline{\text{IRQ}}$ pin low.
1 = $\overline{\text{IRQ}}$ pin high.

XPIN and IPIN are read-only status bits that reflect the logic levels present on the $\overline{\text{XIRQ}}$ and $\overline{\text{IRQ}}$ pins. XPIN and IPIN provide the data bits that allow the $\overline{\text{XIRQ}}$ and $\overline{\text{IRQ}}$ pins to be used as general-purpose inputs. However, to use $\overline{\text{XIRQ}}$ and $\overline{\text{IRQ}}$ as data inputs, the interrupts normally generated by these two pins must be disabled with the DISX and DISI bits in the DDRD register.

After reset PD[1:0] are configured as high-impedance inputs. PD[1:0] share functions with the SCI system. **8 Serial Communications Interface** details information regarding port D SCI functions.

DDRD — Port D Data Direction **$1009**

	BIT 7	6	5	4	3	2	1	BIT 0
	DISX	DISI	—	—	—	—	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0

DISX — Disable $\overline{\text{XIRQ}}$ Pin Interrupts

Can be read anytime. Can be written only once. Any write to the DDRD register will prevent modification of this bit. This bit must be set to use the $\overline{\text{XIRQ}}$ pin as a data input.

0 = Interrupts generated by the $\overline{\text{XIRQ}}$ pin function are enabled
1 = Interrupts generated by the $\overline{\text{XIRQ}}$ pin function are disabled

DISI — Disable $\overline{\text{IRQ}}$ Pin Interrupts

Can be read anytime. Can be written only once. Any write to the DDRD register will prevent modification of this bit. This bit must be set to use the $\overline{\text{IRQ}}$ pin as a data input.

0 = Interrupts generated by the $\overline{\text{IRQ}}$ pin function are enabled
1 = Interrupts generated by the $\overline{\text{IRQ}}$ pin function are disabled

DDD[1:0] — Data Direction for PD[1:0]

0 = Corresponding port D pin configured for input
1 = Corresponding port D pin configured for output

PORTE — Port E Data **$100A**

	BIT 7	6	5	4	3	2	1	BIT 0
	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
RESET:	I	I	I	I	I	I	I	I

Port E has eight general-purpose input pins and shares functions with the A/D converter system. When any port E pins are being used as A/D inputs, PORTE should not be read during the sample portion of an A/D conversion. Refer to **9 Analog-to-Digital Converter** for more information.

7 Timing System

The timing system is based on a free-running 16-bit counter with a four-stage programmable prescaler. A timer overflow function allows software to extend the system's timing capability beyond the counter's 16-bit range. The main timer consists of the timer prescaler, the 16-bit free-running counter, and the capture/compare unit. **7.2 Main Timer** details this portion of the timing system.

The free-running counter can be driven by either the EXTAL signal, as in other M68HC11 derivatives or it can be driven by a software-controlled phase-locked loop (PLL) frequency synthesizer which has been added to the MC68HC(7)11EA9 MCUs. The PLL allows the MCU to operate in WAIT mode with extremely low power requirements. Refer to **7.1 Phase-Locked Loop Synthesizer**.

In addition, the timing system includes pulse accumulator and real-time interrupt (RTI) functions, as well as a clock monitor function, which can be used to detect clock failures that are not detected by the COP system. Refer to the appropriate paragraphs within this section for information regarding these functions. **Table 12** shows a summary of the crystal-related frequencies and periods.

Table 12 Timer Summary

Control Bits	Common System Frequencies			Definition
	4.0 MHz	8.0 MHz	12.0 MHz	XTAL
	1.0 MHz	2.0 MHz	3.0 MHz	E
PR[1:0]	**Main Timer Count Rate (Period Length)**			
0 0				
1 count —	1000 ns	500 ns	333 ns	1/E
overflow —	65.536 ms	32.768 ms	21.845 ms	2^{16}/E
0 1				
1 count —	4.0 µs	2.0 µs	1.333 µs	4/E
overflow —	262.14 ms	131.07 ms	32.768 ms	2^{18}/E
1 0				
1 count —	8.0 µs	4.0 µs	2.667 µs	8/E
overflow —	524.28 ms	262.14 ms	174.76 ms	2^{19}/E
1 1				
1 count —	16.0 µs	8.0 µs	5.333 µs	16/E
overflow —	1.049 s	524.29 ms	349.52 ms	2^{20}/E
RTR[1:0]	**Periodic (RTI) Interrupt Rates (Period Length)**			
0 0	8.192 ms	4.096 ms	2.731 ms	2^{13}/E
0 1	16.384 ms	8.192 ms	5.461 ms	2^{14}/E
1 0	32.768 ms	16.384 ms	10.923 ms	2^{15}/E
1 1	65.536 ms	32.768 ms	21.845 ms	2^{16}/E
CR[1:0]	**COP Watchdog Timeout Rates (Period Length)**			
0 0	32.768 ms	16.384 ms	10.923 ms	2^{15}/E
0 1	131.072 ms	65.536 ms	43.691 ms	2^{17}/E
1 0	524.288 ms	262.14 ms	174.76 ms	2^{19}/E
1 1	2.098 s	1.049 s	699.05 ms	2^{21}/E
Time-out Tolerance (–0 ms/+...)	32.8 ms	16.4 ms	10.9 ms	2^{15}/E

7.1 Phase-Locked Loop Synthesizer

The phase-locked loop synthesizer (PLL) generates clocks for the CPU, bus circuitry, and A/D converter. The clocks for the SCI and timers are derived directly from the EXTAL clock. The EXTAL clock also provides the reference for the synthesizer which generates a frequency that is a multiple of the EXTAL clock frequency. Values written to the SYNR register determine the factor by which the EXTAL clock is scaled. Refer to **Figure 8**.

The PLL has two frequency bandwidths which are automatically selected whenever AUTO = 1 in the PLLCR register. When the PLL is first enabled, the wide bandwidth is selected to provide a fast ramp time. When the desired frequency is nearly reached, the low bandwidth is selected to provide greater stability. Manual control of bandwidth can be accomplished by clearing the AUTO bit.

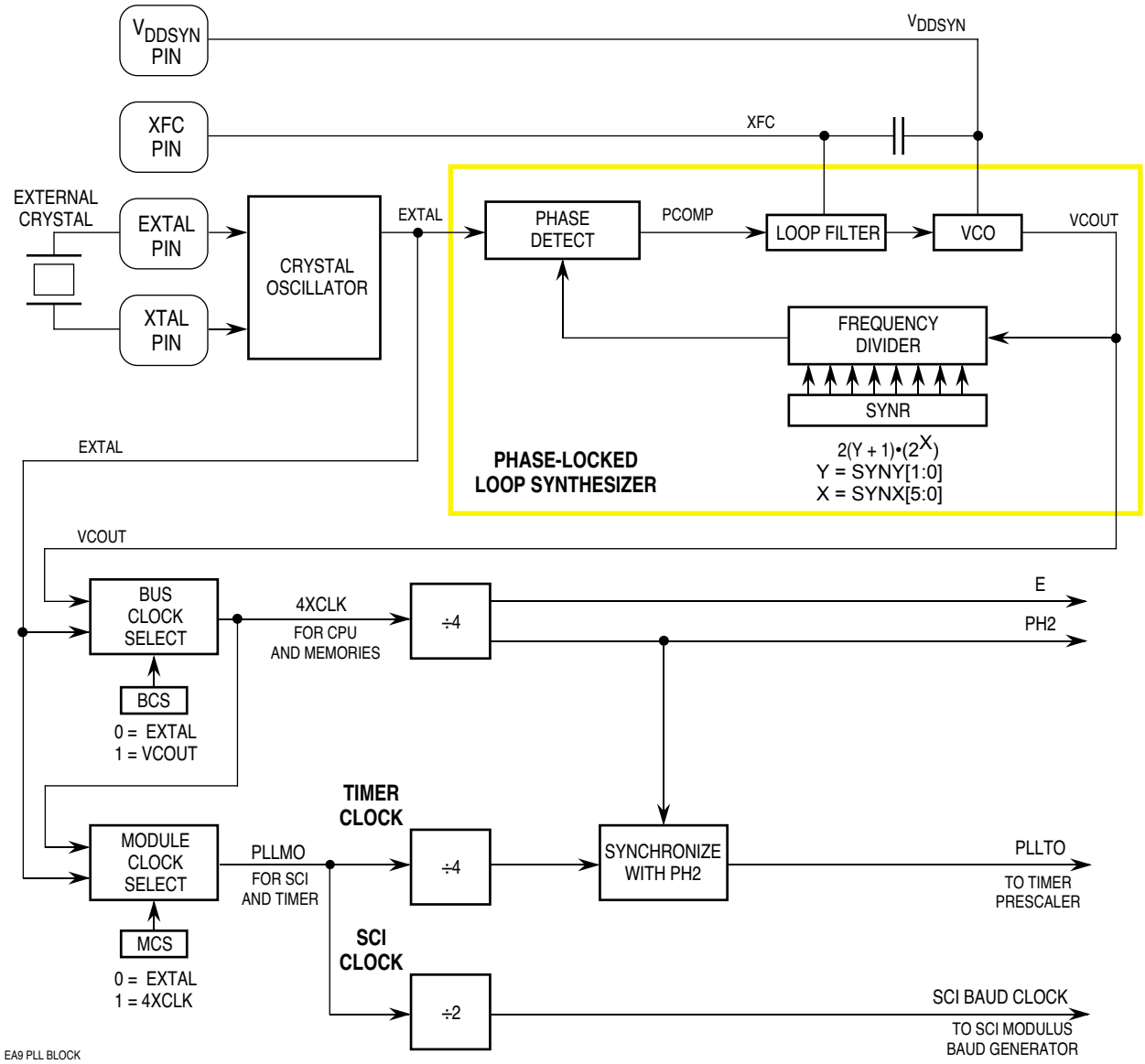


Figure 8 Phase-Locked Loop Synthesizer Block Diagram

PLLCR — PLL Control **$1036**

	BIT 7	6	5	4	3	2	1	BIT 0
	PLLON	BCS	AUTO	BWC	VCOT	MCS	LCK	WEN
RESET:	1	0	1	1	1	0	0	0

PLLON — PLL System Enable

This bit activates the PLL synthesizer circuit without connecting its output to the control circuit. This allows the synthesizer to stabilize before it can drive the CPU clocks. This bit resets to one, allowing the synthesizer to stabilize as the device is being powered up.

0 = PLL is off
1 = PLL is on

BCS — Bus Clock Select

This bit determines which signal drives the clock circuitry generating the bus clocks. Refer to **Figure 8**. Once BCS has been changed, up to 1.5 EXTAL cycles + 1.5 PLLOUT cycles may be required for the transition. During the transition, all CPU activity will cease. BCS is cleared by a STOP or WAIT instruction or when V_{DDSYN} falls to the V_{SS} level.

0 = EXTAL drives the clock circuit
1 = VCOUT drives the clock circuit

NOTE

PLLON and BCS have built-in protection such that the PLL cannot be selected to drive any clocks if the PLL is off. Similarly, the PLL cannot be turned off if it has been selected as a clock source. Turning the PLL on and selecting its output as a clock source require two separate writes to the PLLCR register.

AUTO — Automatic/Manual Loop Filter Bandwidth Control

This bit selects between automatic bandwidth control circuits within the phase detect block and manual bandwidth control. Refer to **Table 13**.

0 = Automatic bandwidth control is selected
1 = Bandwidth control is manual

BWC — Loop Filter Bandwidth Control/Status

Bandwidth control is manual only when AUTO = 0. Since the low bandwidth driver is always enabled, BWC determines if the high bandwidth driver is enabled. When AUTO = 1, BWC is a read-only status bit that indicates which mode has been selected by the internal circuit. During PLL start-up in automatic mode, the high bandwidth driver is enabled by internal circuitry until the PLL is near the selected frequency. The high bandwidth driver is then disabled and BWC is cleared. Refer to **Table 13**.

0 = Only the low bandwidth driver is enabled
1 = Both low and high bandwidth drivers are selected

Table 13 Loop Filter Bandwidth Driver Control

AUTO	BWC	VCOT	High Bandwidth Driver	Low Bandwidth Driver
0	0	0	Off	Off
0	0	1	Off	On
0	1	0	On	Off
0	1	1	On	On
1	X	1	Automatic	On

VCOT — Voltage Controlled Oscillator (VCO) Test

This bit is used to isolate the loop filter from the VCO to aid in factory testing of the PLL. VCOT is always set when AUTO = 1 (automatic bandwidth control mode). This bit can be written only in special test mode.

0 = Loop filter low bandwidth mode is disabled (factory test only)
1 = Loop filter operates according to values of AUTO and BWC control bits

MCS — Module Clock Select

This bit determines which clock signal drives the SCI and timer.

0 = EXTAL is the clock source for SCI and timer divider chains

1 = 4XCLK is the clock source for the SCI and timer divider chains

LCK— Synthesizer Lock Detect Flag

This is a read-only status bit that indicates when the PLL has stabilized. BCS cannot be set (selecting VCOUT as a clock source) until LCK is set.

0 = The PLL is not stable

1 = The PLL has stabilized

WEN — WAIT Enable

This bit determines whether the EXTAL signal will be used to drive the CPU clocks while the device is in WAIT mode. When this feature is enabled, entering wait mode clears BCS (selecting EXTAL as the source for CPU clocks) and reduces the PLL frequency to the lowest value, modulus 1. Any interrupt or reset or the assertion of the RAF bit within the SCI (if the receiver is enabled by RE = 1) will allow the PLL to resume operation at the frequency selected in SYNR register. Then the user must set BCS to select VCOUT as the source for CPU clocks.

0 = VCOUT remains connected to the 4XCLK circuit during operation in WAIT mode.

1 = After stacking prior to entering WAIT mode, BCS is cleared and the PLL is maintained at the lowest frequency available (modulus 1).

SYNR — Frequency Synthesizer Control **$1037**

	BIT 7	6	5	4	3	2	1	BIT 0
	SYNX1	SYNX0	SYNY5	SYNY4	SYNY3	SYNY2	SYNY1	SYNY0
RESET:	0	0	0	0	0	1	1	0

This register resets to $06 for a preset multiplication factor of 14.

SYNX[1:0] — Binary Tap Select Bits

These two bits select one of four binary taps. SYNX[1:0] affect the frequency multiplication factor, variable *X* according to the formula below.

SYNY[5:0] — Modulo Counter Rate Select Bits

These six bits select one of 64 binary values that affect the frequency multiplication factor, variable *Y* according to the formula below.

$$2 \cdot (Y + 1) \cdot (2^X)$$

Where

X = the value represented by bits SYNX[1:0]

Y = the value represented by bits SYNY[5:0]

7.2 Main Timer

The main timer consists of the timer prescaler, the free-running counter, and the capture/compare unit. The timer prescaler selects one of four division rates and drives the free-running 16-bit counter. The capture/compare unit has three channels for input capture, four channels for output compare, and one channel that can be configured as a fourth input capture or a fifth output compare. Timer channels configured for input capture (ICx) cause the current value of the free-running counter to be latched into an input capture register (TICx) when a pulse edge is detected on the corresponding pin. Channels configured for output compare allow a pulse to be output when the free-running counter matches a value loaded into an output compare register (TOCx). **Figure 9** shows a detailed block diagram of the timer prescaler and the capture/compare unit.

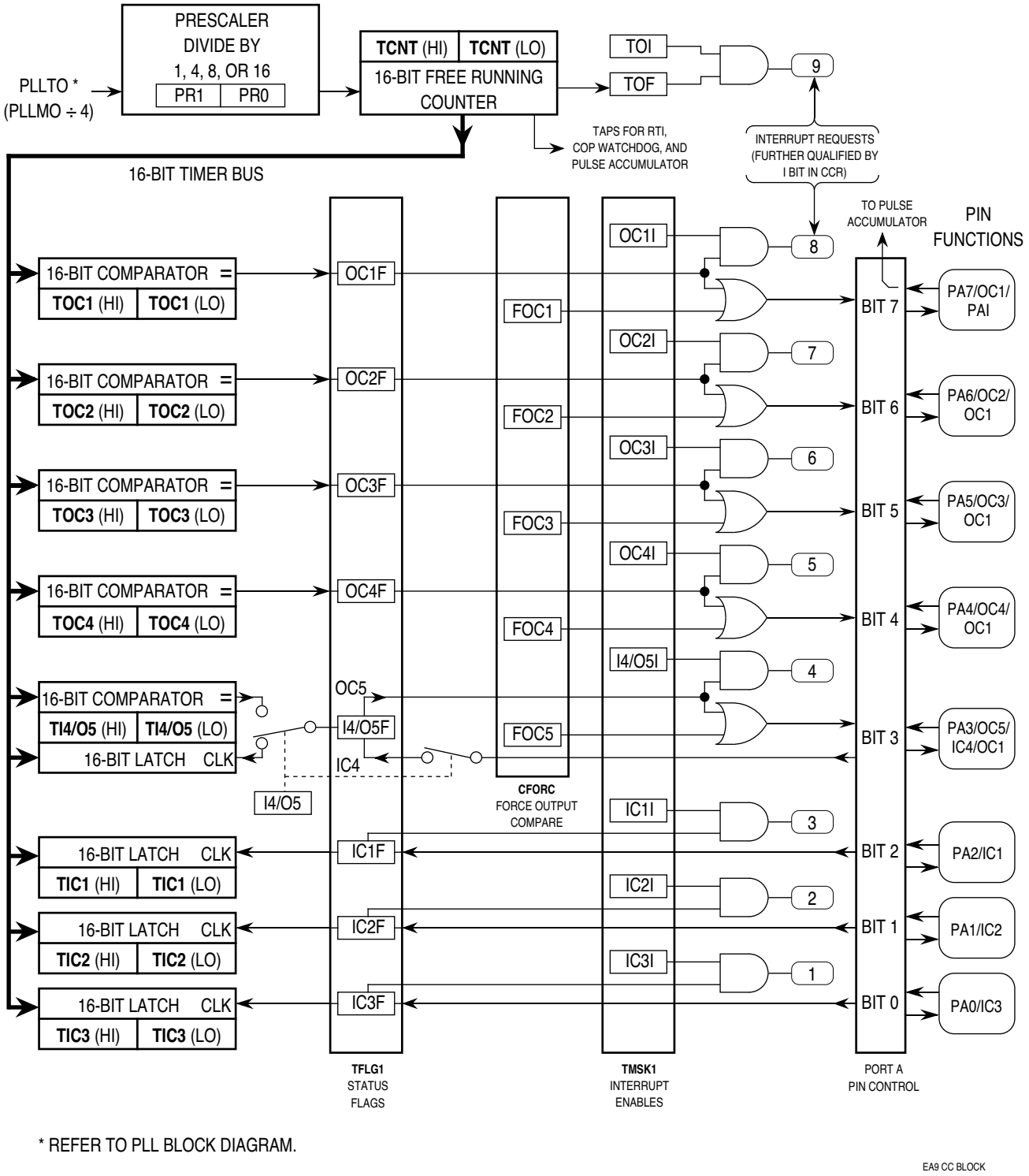


Figure 9 Main Timer Block Diagram

CFORC — Timer Compare Force **$100B**

	BIT 7	6	5	4	3	2	1	BIT 0
	FOC1	FOC2	FOC3	FOC4	FOC5	—	—	—
RESET:	0	0	0	0	0	0	0	0

FOC[1:5] — Force Output Compare
Write ones to force compare(s)
0 = Not affected
1 = Output x action occurs

Bits [2:0] — Not implemented
Always read zero

OC1M — Output Compare 1 Mask **$100C**

	BIT 7	6	5	4	3	2	1	BIT 0
	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	—	—	—
RESET:	0	0	0	0	0	0	0	0

Set bit(s) to enable OC1 to control corresponding port A pin(s). If OC1Mx is set, data in OC1Dx is output on port A pin x upon successful OC1 compares.

Bits [2:0] — Not implemented
Always read zero

OC1D — Output Compare 1 Data **$100D**

	BIT 7	6	5	4	3	2	1	BIT 0
	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	—	—	—
RESET:	0	0	0	0	0	0	0	0

Set bit(s) to enable OC1 to control corresponding port A pin(s). If OC1Mx is set, data in OC1Dx is output to port A bit x on successful OC1 compares.

Bits [2:0] — Not implemented
Always read zero

TCNT — Timer Counter **$100E–$100F**

BIT 15	14	13	12	11	10	9	BIT 8	TCNT (HI)
BIT 7	6	5	4	3	2	1	BIT 0	TCNT (LO)

TCNT resets to $0000. In normal modes (SMOD = 0), TCNT is a read-only register.

TIC1–TIC3 — Timer Input Capture **$1010–$1015**

$1010	BIT 15	14	13	12	11	10	9	BIT 8	TIC1 (HI)
$1011	BIT 7	6	5	4	3	2	1	BIT 0	TIC1 (LO)
$1012	BIT 15	14	13	12	11	10	9	BIT 8	TIC2 (HI)
$1013	BIT 7	6	5	4	3	2	1	BIT 0	TIC2 (LO)
$1014	BIT 15	14	13	12	11	10	9	BIT 8	TIC3 (HI)
$1015	BIT 7	6	5	4	3	2	1	BIT 0	TIC3 (LO)

TICx is not affected by reset.

TOC1–TOC4 — Timer Output Compare **$1016–$101D**

$1016	BIT 15	14	13	12	11	10	9	BIT 8	TOC1 (HI)
$1017	BIT 7	6	5	4	3	2	1	BIT 0	TOC1 (LO)
$1018	BIT 15	14	13	12	11	10	9	BIT 8	TOC2 (HI)
$1019	BIT 7	6	5	4	3	2	1	BIT 0	TOC2 (LO)
$101A	BIT 15	14	13	12	11	10	9	BIT 8	TOC3 (HI)
$101B	BIT 7	6	5	4	3	2	1	BIT 0	TOC3 (LO)
$101C	BIT 15	14	13	12	11	10	9	BIT 8	TOC4 (HI)
$101D	BIT 7	6	5	4	3	2	1	BIT 0	TOC4 (LO)

All TOCx register pairs reset to $FFFF.

TI4/O5 — Timer Input Capture 4/Output Compare 5 **$101E–$101F**

BIT 15	14	13	12	11	10	9	BIT 8	TCNT (HI)
BIT 7	6	5	4	3	2	1	BIT 0	TCNT (LO)

This is a shared register and is either input capture 4 or output compare 5 depending on the state of bit I4/O5 in PACTL. Writes to TI4/O5 have no effect when this register is configured as input capture 4. The TI4/O5 register pair resets to $FFFF.

TCTL1 — Timer Control 1 **$1020**

	BIT 7	6	5	4	3	2	1	BIT 0
	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
RESET:	0	0	0	0	0	0	0	0

Table 14 Output Compare Channel Configuration

OMx	OLx	Action on Successful Compare
0	0	None — Output Compare Channel (OCx) disabled
0	1	Toggle OCx output pin logic level
1	0	Drive OCx output pin low
1	1	Drive OCx output pin high

TCTL2 — Timer Control 2 **$1021**

	BIT 7	6	5	4	3	2	1	BIT 0
	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
RESET:	0	0	0	0	0	0	0	0

Table 15 Input Capture Channel Configuration

EDGxB	EDGxA	Input Capture Configuration
0	0	Input Capture Channel (ICx) disabled
0	1	Capture on rising edge on ICx input pin
1	0	Capture on falling edge on ICx input pin
1	1	Capture on any edge on ICx input pin

TMSK1 — Timer Interrupt Mask 1 **$1022**

	BIT 7	6	5	4	3	2	1	BIT 0
	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I
RESET:	0	0	0	0	0	0	0	0

OC1I–OC4I — Output Compare (OCx) Interrupt Enable

If the OCxI enable bit is set when a match occurs, an interrupt is generated.

0 = Interrupts from OCx channel disabled

1 = Successful compares on OCx channel generate interrupts

I4/O5I — Input Capture 4/Output Compare 5 Interrupt Enable

When I4/O5 in PACTL is one, I4/O5I is the input capture 4 interrupt enable bit and edges on the I4/O5 pin generate interrupts. When I4/O5 in PACTL is zero, I4/O5I is the output compare 5 interrupt enable bit and successful matches generate interrupts.

0 = Interrupts from IC4/OC5 channel disabled

1 = Interrupts from IC4/OC5 channel enabled

IC1I–IC3I — Input Capture (ICx) Interrupt Enable

If the ICxI enable bit is set when an edge is detected on the ICx pin, an interrupt is generated.

0 = Interrupts from ICx channel disabled

1 = Edges detected on ICx pin generate interrupts

NOTE

Bits in TMSK1 correspond bit for bit with flag bits in TFLG1. Ones in TMSK1 enable the corresponding interrupt sources.

TFLG1 — Timer Interrupt Flag 1 **$1023**

	BIT 7	6	5	4	3	2	1	BIT 0
	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F
RESET:	0	0	0	0	0	0	0	0

Clear a flag by writing a one to the appropriate bit.

OC1F–OC4F — Output Compare (OCx) Interrupt Flag

If the OCxI enable bit is set when a match occurs, the corresponding flag bit is set and an interrupt is generated.

0 = No match has occurred

1 = A successful compare has occurred on OCx channel

I4/O5I — Input Capture 4/Output Compare 5 Interrupt Enable

When I4/O5 in PACTL is one, I4/O5I is the input capture 4 interrupt enable bit and edges (rising or falling, depending on configuration) on the I4/O5 pin cause this flag to be set and an interrupt is generated. When I4/O5 in PACTL is zero, I4/O5I is the output compare 5 interrupt enable bit and successful matches cause this flag to be set and an interrupt generated.

0 = Interrupts from IC4/OC5 channel disabled

1 = Interrupts from IC4/OC5 channel enabled

IC1I–IC3I — Input Capture (ICx) Interrupt Enable

If the ICxI enable bit is set when an edge (rising or falling, depending on configuration) is detected on the ICx pin, an interrupt is generated.

0 = Interrupts from ICx channel disabled

1 = Edges detected on ICx pin generate interrupts

TMSK2 — Timer Interrupt Mask 2 **$1024**

	BIT 7	6	5	4	3	2	1	BIT 0
	TOI	RTII	PAOVI	PAII	—	—	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

Bits [7:4] can be written at any time. PR[1:0] can only be written once in the first 64 cycles after reset in normal modes (SMOD = 0). In special modes (SMOD = 1) PR[1:0] can be written any time.

TOI — Timer Overflow Interrupt Enable

If the TOI enable bit is set when the value in the timer counter register (TCNT) changes from $FFFF to $0000, an interrupt is generated.

0 = Timer overflow interrupts disabled
1 = Interrupts are generated each time TCNT rolls over to $0000

RTII — Real-Time Interrupt Enable

If RTII enable bit is set, interrupts are generated at the rate determined by the real-time interrupt rate (RTR[1:0]) bits in PACTL.

0 = Periodic interrupts are disabled
1 = Interrupts are generated at the rate determined by RTR[1:0]

PAOVI — Pulse Accumulator Overflow Interrupt Enable

If the PAOVI enable bit is set when the pulse accumulator counter register (PACNT) changes from $FFFF to $0000 an interrupt is generated.

0 = PCNT overflow interrupts are disabled
1 = Interrupts are generated each time PCNT rolls over to $0000

PAII — Pulse Accumulator Input Edge Interrupt Enable

If the PAII enable bit is set when an edge (rising or falling, depending on configuration) is detected on the pulse accumulator input pin (PA7/PAI), an interrupt is generated.

0 = Interrupts from edges on PAI pin are disabled
1 = Edges detected on PAI pin generate interrupts (rising or falling, depending on configuration)

Bits [3:2] — Not Implemented

Always read zero

PR[1:0] — Timer Prescaler Select

Table 16 Main Timer Prescaler Selection

PR1	PR0	Prescaler Selected
0	0	÷1
0	1	÷4
1	0	÷8
1	1	÷16

TFLG2 — Timer Interrupt Flag 2 **$1025**

	BIT 7	6	5	4	3	2	1	BIT 0
	TOF	RTIF	PAOVF	PAIF	—	—	—	—
RESET:	0	0	0	0	0	0	0	0

TOF — Timer Overflow Interrupt Flag

If the TOI enable bit is set when the timer counter register (TCNT) changes from $FFFF to $0000, this flag is set and an interrupt is generated.

0 = TCNT has not rolled over since either the TOF flag bit was last cleared or the TOI enable bit was set.

1 = TCNT has rolled over to $0000

RTIF — Real-Time Interrupt Flag

If RTII enable bit is set, this flag is set and an interrupt is generated periodically at the rate determined by the real-time interrupt rate (RTR[1:0]) bits in PACTL.

0 = No periodic interrupt has occurred since either the RTIF flag bit was last cleared or when the RTII enable bit was set

1 = A periodic interrupt has occurred

PAOVF — Pulse Accumulator Overflow Interrupt Flag

If the PAOVI enable bit is set when the pulse accumulator counter register (PCNT) rolls over to $0000, this flag is set and an interrupt is generated.

0 = PCNT has not rolled over since either the PAOVF flag bit was last cleared or the PAOVI enable bit was set.

1 = PCNT has rolled over to $0000

PAIF — Pulse Accumulator Input Edge Interrupt Flag

If the PAII enable bit is set when an edge is detected on the pulse accumulator input pin (PA7/PAI), this flag is set and an interrupt is generated.

0 = No edge has been detected on the PAI pin

1 = An edge (rising or falling, depending on configuration) has been detected on the PAI pin

Bits [3:0] — Not Implemented

Always read zero

PACTL — Pulse Accumulator Control **$1026**

	BIT 7	6	5	4	3	2	1	BIT 0
	—	PAEN	PAMOD	PEDGE	—	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

Bits [7:4] can be written at any time. PR[1:0] can only be written once in the first 64 cycles after reset in normal modes (SMOD = 0). In special modes (SMOD = 1) PR[1:0] can be written any time.

Bit 7 — Not Implemented

Always reads zero

PAEN — Pulse Accumulator Enable

Refer to **7.4 Pulse Accumulator**.

PAMOD — Pulse Accumulator Mode Select

Refer to **7.4 Pulse Accumulator**.

PEDGE — Pulse Accumulator Input Edge Select

Refer to **7.4 Pulse Accumulator**.

Bit 3 — Not Implemented
Always reads zero

I4/O5 — Input Capture 4/Output Compare 5 Select
0 = Interrupts from edges on PAI pin are disabled
1 = Edges detected on PAI pin generate interrupts (rising or falling, depending on configuration)

RTR[1:0] — Real-Time Interrupt Rate Select

Table 17 Real-Time Interrupt Rates

RTR[1:0]	Rate Selected	RTI Rate Selected		
		E = 1.0 MHz	E = 2.0 MHz	E = 3.0 MHz
0 0	$2^{13} \div E$	8.192 ms	4.096 ms	2.731 ms
0 1	$2^{14} \div E$	16.384 ms	8.192 ms	5.461 ms
1 0	$2^{15} \div E$	32.768 ms	16.384 ms	10.923 ms
1 1	$2^{16} \div E$	65.536 ms	32.768 ms	21.845 ms

OPTION — System Configuration Options **$1039**

	BIT 7	6	5	4	3	2	1	BIT 0
	ADPU	CSEL	IRQE*	DLY*	CME	—	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

* Can be written only once in first 64 cycles after reset in normal modes, or at any time in special modes.

ADPU — A/D Converter Power up
Refer to **9 Analog-to-Digital Converter**

CSEL — Clock Select
0 = A/D and EEPROM use the system E clock
1 = A/D and EEPROM use internal RC clock

IRQE — $\overline{\text{IRQ}}$ Select Edge-Sensitive Only
Refer to **5 Resets and Interrupts**

DLY — Enable Oscillator Start-up Delay
0 = No stabilization delay on exit from STOP mode.
1 = A delay of approximately 4000 E-clock cycles is imposed as the MCU exits STOP mode.

CME — Clock Monitor Enable
0 = Clock monitor disabled; slow clock can be used.
1 = Slow or stopped clocks cause COP failure reset.

Bit 2 — Not implemented
Always reads zero

CR[1:0] — COP Timer Rate Select
Refer to **5 Resets and Interrupts**

Table 18 COP Timer Rate Selection

CR[1:0]	Rate Selected	Period Length		
		E = 1.0 MHz	E = 2.0 MHz	E = 3.0 MHz
0 0	$2^{15} \div E$	32.768 ms	16.384 ms	10.923 ms
0 1	$2^{17} \div E$	131.072 ms	65.536 ms	43.691 ms
1 0	$2^{19} \div E$	524.288 ms	262.140 ms	174.76 ms
1 1	$2^{21} \div E$	2.097 s	1.049 s	699.05 ms

7.3 Real-Time Interrupt

The real-time interrupt (RTI) function can generate interrupts at different fixed periodic rates. These rates are a function of the MCU oscillator frequency and the value of the software-accessible control bits, RTR1 and RTR0. These bits determine the rate at which interrupts are requested by the RTI system. The RTI system is driven by an E divided by 2^{13} rate clock compensated so that it is independent of the timer prescaler. The RTR1 and RTR0 control bits select an additional division factor. RTI is set to its fastest rate by default out of reset and can be changed at any time.

Table 19 Real-Time Interrupt Rates (Period Length)

RTR[1:0]	Period Length Selected	Period Length		
		E = 1.0 MHz	E = 2.0 MHz	E = 3.0 MHz
0 0	$2^{13} \div E$	8.192 ms	4.096 ms	2.731 ms
0 1	$2^{14} \div E$	16.384 ms	8.192 ms	5.461 ms
1 0	$2^{15} \div E$	32.768 ms	16.384 ms	10.923 ms
1 1	$2^{16} \div E$	65.536 ms	32.768 ms	21.845 ms

Table 20 Real-Time Interrupt Rates (Frequency)

RTR[1:0]	Maximum Frequency Possible	Maximum Interrupt Frequency		
		E = 1.0 MHz	E = 2.0 MHz	E = 3.0 MHz
0 0	$2^{13} \div E$	122.070 Hz	244.141 Hz	366.211 Hz
0 1	$2^{14} \div E$	61.035 Hz	122.070 Hz	183.105 Hz
1 0	$2^{15} \div E$	30.518 Hz	61.035 Hz	91.553 Hz
1 1	$2^{16} \div E$	15.258 Hz	30.518 Hz	45.776 Hz

TFLG2 — Timer Interrupt Flag 2 **$1025**

	BIT 7	6	5	4	3	2	1	BIT 0
	TOF	RTIF	PAOVF	PAIF	—	—	—	—
RESET:	0	0	0	0	0	0	0	0

TOF — Timer Overflow Interrupt Flag
Refer to **7.2 Main Timer**

RTIF — Real-Time Interrupt Flag
If RTII enable bit is set, this flag is set and an interrupt is generated periodically at the rate determined by the real-time interrupt rate (RTR[1:0]) bits in PACTL.
0 = No periodic interrupt has occurred since either the RTIF flag bit was last cleared or the RTII enable bit was set
1 = A periodic interrupt has occurred

PAOVF — Pulse Accumulator Overflow Interrupt Flag
Refer to **7.4 Pulse Accumulator**

PAIF — Pulse Accumulator Input Edge Interrupt Flag
Refer to **7.4 Pulse Accumulator**

Bits [3:0] — Not Implemented
Always read zero

PACTL — Pulse Accumulator Control **$1026**

	BIT 7	6	5	4	3	2	1	BIT 0
	—	PAEN	PAMOD	PEDGE	—	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

Bits [7:4] can be written at any time. PR[1:0] can only be written once in the first 64 cycles after reset in normal modes (SMOD = 0). In special modes (SMOD = 1) PR[1:0] can be written any time.

Bit 7 — Not Implemented
Always reads zero

PAEN — Pulse Accumulator Enable
Refer to **7.4 Pulse Accumulator**

PAMOD — Pulse Accumulator Mode Select
Refer to **7.4 Pulse Accumulator**

PEDGE — Pulse Accumulator Input Edge Select
Refer to **7.4 Pulse Accumulator**

Bit 3 — Not Implemented
Always reads zero

I4/O5 — Input Capture 4/Output Compare 5 Select
Refer to **7.2 Main Timer**

RTR[1:0] — Real-Time Interrupt Rate Select

Table 21 Real-Time Interrupt Rates

RTR[1:0]	Rate Selected	RTI Rate Selected		
		E = 1.0 MHz	E = 2.0 MHz	E = 3.0 MHz
0 0	$2^{13} \div E$	8.192 ms	4.096 ms	2.731 ms
0 1	$2^{14} \div E$	16.384 ms	8.192 ms	5.461 ms
1 0	$2^{15} \div E$	32.768 ms	16.384 ms	10.923 ms
1 1	$2^{16} \div E$	65.536 ms	32.768 ms	21.845 ms

7.4 Pulse Accumulator

M68HC11-family MCUs have an 8-bit counter within the timing system that can be configured for event counting or for gated time accumulation. The counter (PACNT) can be read or written at any time.

The port A bit 7 I/O pin can be configured to act as a clock in event counting mode and edges on the pulse accumulator input pin cause the counter (PACNT) to increment. When the pulse accumulator is configured for time accumulation, an edge on the pulse accumulator input pin enables a free-running clock (E divided by 64) that drives PACNT in gated time accumulation mode. Refer to **Figure 10**.

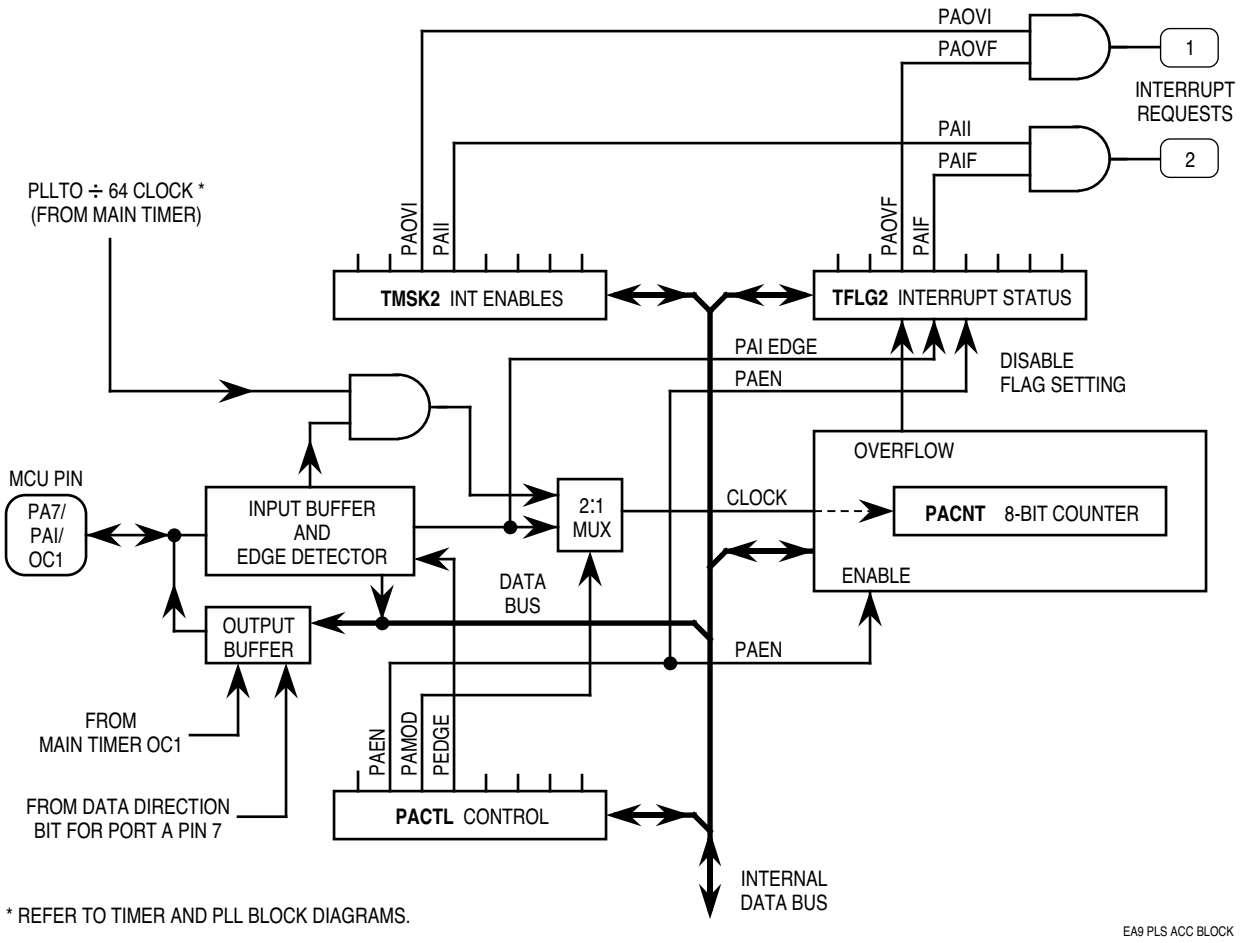


Figure 10 Pulse Accumulator Block Diagram

PACTL — Pulse Accumulator Control **$1026**

	BIT 7	6	5	4	3	2	1	BIT 0
	—	PAEN	PAMOD	PEDGE	—	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

Bits [7:4] can be written at any time. PR[1:0] can only be written once in the first 64 cycles after reset in normal modes (SMOD = 0). In special modes (SMOD = 1) PR[1:0] can be written any time.

Bit 7 — Not Implemented
Always reads zero

PAEN — Pulse Accumulator Enable
0 = Periodic interrupts are disabled
1 = Interrupts are generated at the rate determined by RTR[1:0]

PAMOD — Pulse Accumulator Mode Select
0 = PCNT overflow interrupts are disabled
1 = Interrupts are generated each time PCNT rolls over to $0000

PEDGE — Pulse Accumulator Input Edge Select
0 = Interrupts from edges on PAI pin are disabled
1 = Edges detected on PAI pin generate interrupts (rising or falling, depending on configuration)

Bit 3 — Not Implemented
Always reads zero

I4/O5 — Input Capture 4/Output Compare 5 Select
Refer to **7.2 Main Timer**.

RTR[1:0] — Timer Prescaler Select
Refer to **7.3 Real-Time Interrupt**.

PACNT — Pulse Accumulator Counter **$1027**

	BIT 7	6	5	4	3	2	1	BIT 0
	BIT 7	6	5	4	3	2	1	BIT 0

Can be read and written, unaffected by reset.

TMSK2 — Timer Interrupt Mask 2 **$1024**

	BIT 7	6	5	4	3	2	1	BIT 0
	TOI	RTII	PAOVI	PAII	—	—	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

Bits [7:4] can be written at any time. PR[1:0] can only be written once in the first 64 cycles after reset in normal modes (SMOD = 0). In special modes (SMOD = 1) PR[1:0] can be written any time.

TOI — Timer Overflow Interrupt Enable
Refer to **7.2 Main Timer**.

RTII — Real-Time Interrupt Enable
Refer to **7.3 Real-Time Interrupt**.

PAOVI — Pulse Accumulator Overflow Interrupt Enable
If the PAOVI enable bit is set when the pulse accumulator counter register (PACNT) changes from $FFFF to $0000 an interrupt is generated.
0 = PCNT overflow interrupts are disabled
1 = Interrupts are generated each time PCNT rolls over to $0000

PAII — Pulse Accumulator Input Edge Interrupt Enable
If the PAII enable bit is set when an edge (rising or falling, depending on configuration) is detected on the pulse accumulator input pin (PA7/PAI), an interrupt is generated.
0 = Interrupts from edges on PAI pin are disabled
1 = Edges detected on PAI pin generate interrupts (rising or falling, depending on configuration)

Bits [3:2] — Not Implemented
Always read zero

PR[1:0] — Timer Prescaler Select
Refer to **7.2 Main Timer**.

TFLG2 — Timer Interrupt Flag 2 **$1025**

	BIT 7	6	5	4	3	2	1	BIT 0
	TOF	RTIF	PAOVF	PAIF	—	—	—	—
RESET:	0	0	0	0	0	0	0	0

TOF — Timer Overflow Interrupt Flag
Refer to **7.2 Main Timer**.

RTIF — Real-Time Interrupt Flag
Refer to **7.3 Real-Time Interrupt**.

PAOVF — Pulse Accumulator Overflow Interrupt Flag
If the PAOVI enable bit is set when the pulse accumulator counter register (PCNT) rolls over to $0000, this flag is set and an interrupt is generated.
0 = PCNT has not rolled over since either the PAOVF flag bit was last cleared or when the PAOVI enable bit was set.
1 = PCNT has rolled over to $0000

PAIF — Pulse Accumulator Input Edge Interrupt Flag
If the PAII enable bit is set when an edge is detected on the pulse accumulator input pin (PA7/PAI), this flag is set and an interrupt is generated.
0 = No edge has been detected on the PAI pin
1 = An edge (rising or falling, depending on configuration) has been detected on the PAI pin

Bits [3:0] — Not Implemented
Always read zero

8 Serial Communications Interface

The SCI, a universal asynchronous receiver transmitter (UART) serial communications interface, is an independent serial I/O subsystem in MC68HC(7)11EA9 MCUs. The registers and control bits used in previous M68HC11 SCI systems have been rearranged and new features added. New or enhanced features include the following:

- A 13-bit modulus prescaler that allows greater baud rate control
- A new idle mode detect, independent of preceding serial data
- A receiver active flag
- Hardware parity for both transmitter and receiver

The enhanced baud rate generator is shown in the following diagram. Refer to the table of SCI baud rate control values for standard values.

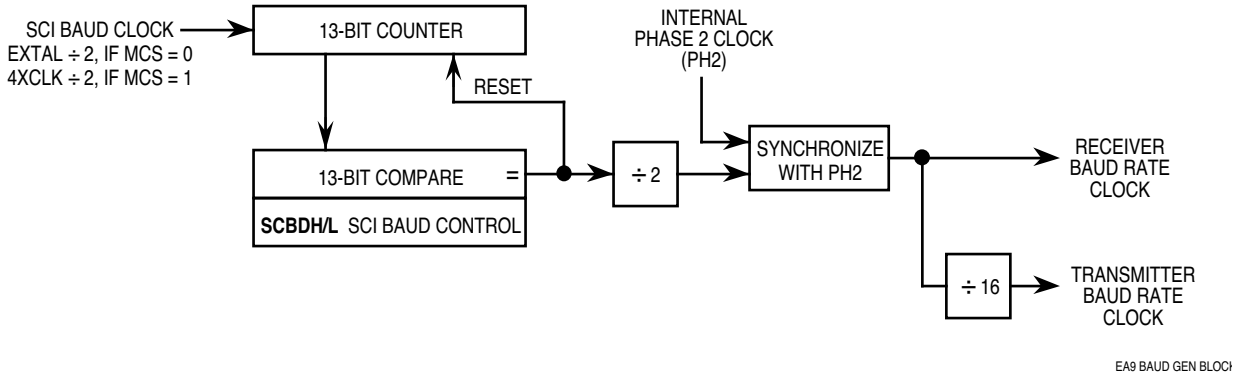


Figure 11 SCI Baud Generator Circuit Diagram

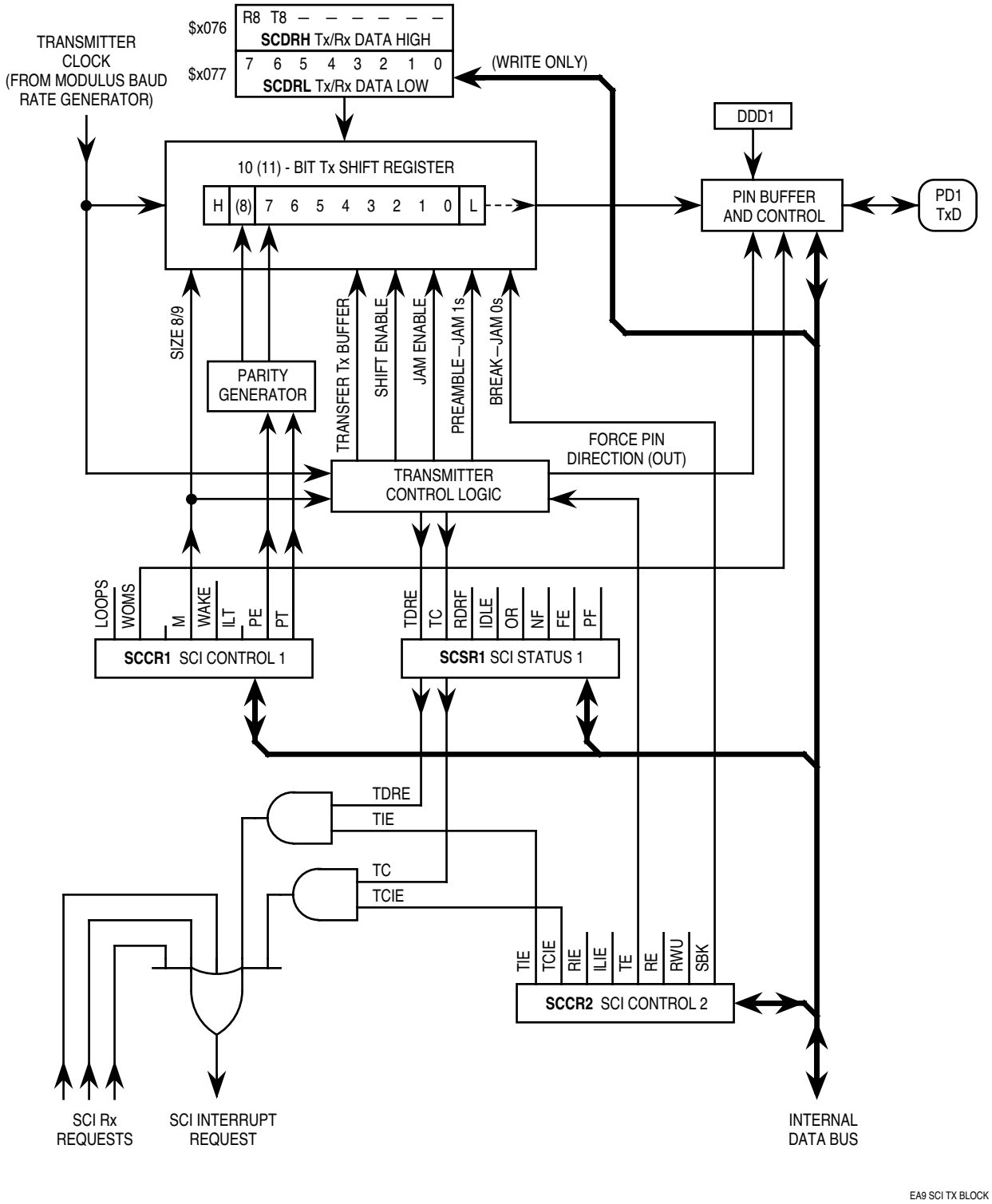


Figure 12 SCI Transmitter Block Diagram

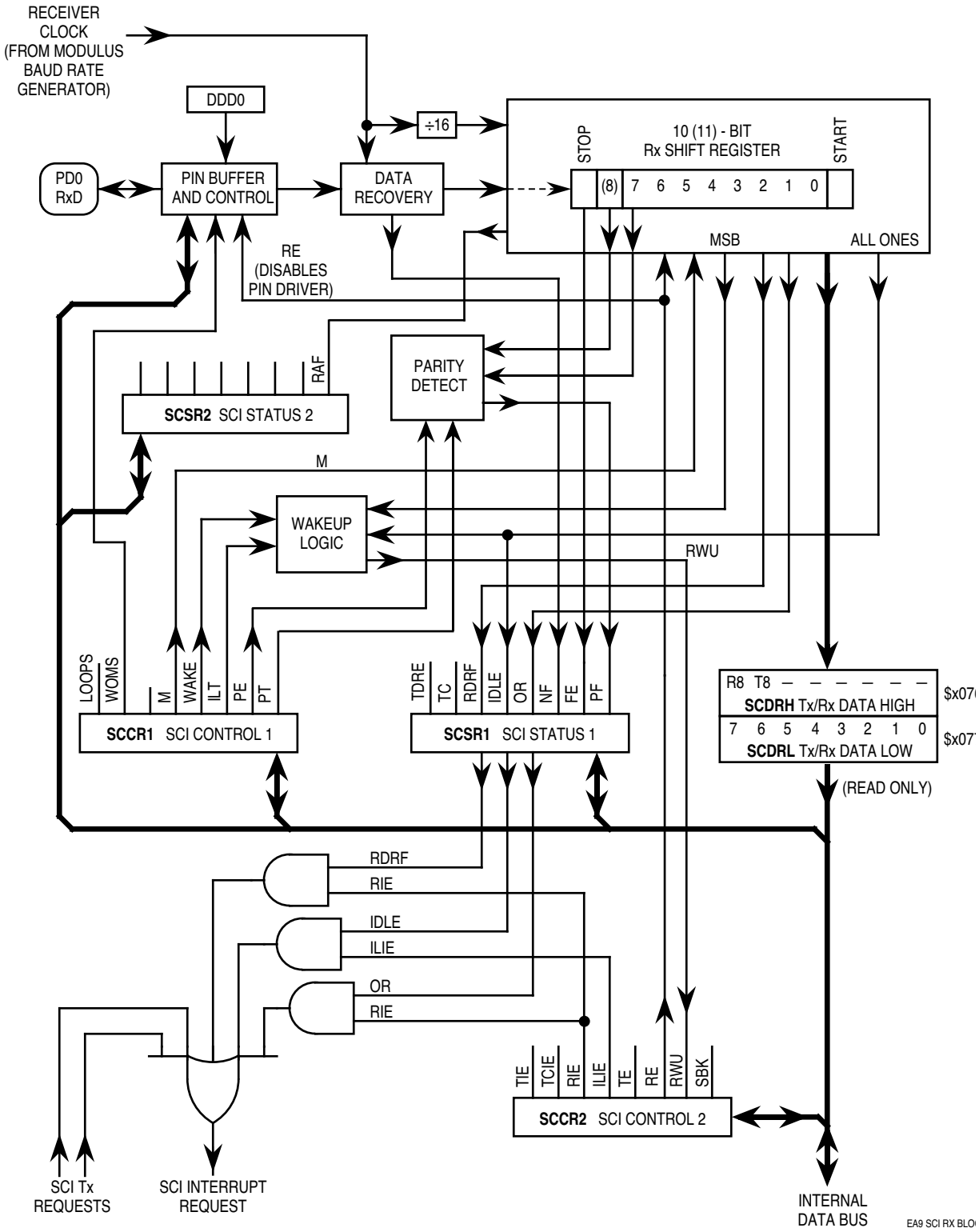


Figure 13 SCI Receiver Block Diagram

SCBDH, SCBDL — SCI Baud Rate Select High, SCI Baud Rate Select Low **$1028, $1029**

	BIT 7	6	5	4	3	2	1	BIT 0	
$1028	BTST	BSPL	—	SBR12	SBR11	SBR10	SBR9	SBR8	High
RESET:	0	0	0	0	0	0	0	0	
$1029	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	Low
RESET:	0	0	0	0	0	1	0	0	

BTST — Baud Register Test (TEST)
Factory test only

BSPL — Baud Rate Counter Split (TEST)
Factory test only

Bit 5 — Not implemented
Always reads zero

SBR[12:0] — SCI Baud Rate Select Bits

Use the following formula to calculate SCI baud rate. Refer to the table of baud rate control values for example rates:

SCI baud rate = EXTAL ÷ (32 • BR)

where BR is the contents of SBR[12:0] in SCBDH,L (BR = 1, 2, 3 ... 8191 decimal, or BR = $0001, $0002, $0003 ... $1FFF hexadecimal)

BR = 0 disables the baud rate generator.

Table 22 Baud Rate Selection

Target Baud Rate	Crystal Frequency (XTAL)					
	8 MHz		12 MHz		16 MHz	
	Dec Value	Hex Value	Dec Value	Hex Value	Dec Value	Hex Value
110	2272	$08E0	3409	$0D51	4545	$11C1
312	156	78	2500	$09C4	3333	$0D05
300	833	$0341	1250	$04E2	1666	$0682
600	416	$01A0	625	$0271	833	$0341
1200	208	$00D0	312	$0138	416	$01A0
2400	104	$0068	156	$009C	208	$00D0
4800	52	$0034	78	$004E	104	$0068
9600	26	$001A	39	$0027	52	$0034
19.2K	13	$000D	20	$0014	26	$001A
38.4K	—	—	—	—	13	$000D

SCCR1 — SCI Control Register 1 **$102A**

	BIT 7	6	5	4	3	2	1	BIT 0
	LOOPS	WOMS	—	M	WAKE	ILT	PE	PT
RESET:	0	0	0	0	0	0	0	0

LOOPS — SCI LOOP Mode Enable
0 = SCI transmit and receive operate normally
1 = SCI transmit and receive are disconnected from TxD and RxD pins, and transmitter output is fed back into the receiver input

WOMS — Wired-Or Mode Option for PD[1:0] (See also DWOM bit in SPCR.)
0 = TxD and RxD operate normally
1 = TxD and RxD are open drains if operating as an output

Bit 5 — Not implemented
Always reads zero

M — Mode (Select Character Format)
0 = Start, 8 data bits, 1 stop bit
1 = Start, 9 data bits, 1 stop bit

WAKE — Wake-Up by Address Mark/Idle
0 = Wake-up by IDLE line recognition
1 = Wake-up by address mark (most significant data bit set)

ILT — Idle Line Type
0 = Short (SCI counts consecutive ones after start bit)
1 = Long (SCI counts ones only after stop bit)

PE — Parity Enable
0 = Parity disabled
1 = Parity enabled

PT — Parity Type
0 = Parity even (even number of ones causes parity bit to be zero, odd number of ones causes parity bit to be one)
1 = Parity odd (odd number of ones causes parity bit to be zero, even number of ones causes parity bit to be one)

SCCR2 — SCI Control Register 2 **$102B**

	BIT 7	6	5	4	3	2	1	BIT 0
	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET:	0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
0 = TDRE interrupts disabled
1 = SCI interrupt requested when TDRE status flag is set

TCIE — Transmit Complete Interrupt Enable
0 = TC interrupts disabled
1 = SCI interrupt requested when TC status flag is set

RIE — Receiver Interrupt Enable
0 = RDRF and OR interrupts disabled
1 = SCI interrupt requested when RDRF flag or the OR status flag is set

ILIE — Idle Line Interrupt Enable
0 = IDLE interrupts disabled
1 = SCI interrupt requested when IDLE status flag is set

TE — Transmitter Enable
0 = Transmitter disabled
1 = Transmitter enabled

RE — Receiver Enable
0 = Receiver disabled
1 = Receiver enabled

RWU — Receiver Wake-Up Control
0 = Normal SCI receiver
1 = Wake-up enabled and receiver interrupts inhibited

SBK — Send Break
0 = Break generator off
1 = Break codes generated as long as SBK = 1

SCSR1 — SCI Status Register 1 **$102C**

	BIT 7	6	5	4	3	2	1	BIT 0
	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
RESET:	0	0	0	0	0	0	0	0

TDRE — Transmit Data Register Empty Flag
Set if transmit data can be written to SCDR; if TDRE = 0, transmit data register is busy. Cleared by SCSR1 read with TDRE set, followed by SCDR write.
0 = Transmit data register contains data and is busy
1 = Transmit data register is empty and SCDR can be written

TC — Transmit Complete Flag
Set if transmitter is idle (no data, preamble, or break transmission in progress). Cleared by SCSR1 read with TC set, followed by SCDR write.
0 = Transmitter is busy
1 = Transmitter is idle and SCDR can be written

RDRF — Receive Data Register Full Flag
Set if a received character is ready to be read from SCDR. Cleared by SCSR1 read with RDRF set, followed by SCDR read.

IDLE — Idle Line Detected Flag
Once cleared, IDLE is set again until the RxD line has been active and becomes idle once more. IDLE flag is inhibited when RWU = 1. Set if the RxD line is idle. Cleared by SCSR1 read with IDLE set, followed by SCDR read.

OR — Overrun Error Flag
Set if a new character is received before a previously received character is read from SCDR. Cleared by SCSR1 read with OR set, followed by SCDR read.

NF — Noise Error Flag
Set if majority sample logic detects anything other than a unanimous decision. Cleared by SCSR1 read with NF set, followed by SCDR read.

FE — Framing Error
Set if a zero is detected where a stop bit was expected. Cleared by SCSR1 read with FE set, followed by SCDR read.

PF — Parity Error Flag
Set if received data has incorrect parity. Cleared by SCSR1 read with PE set, followed by SCDR read.

SCSR2 — SCI Status Register 2 **$102D**

	BIT 7	6	5	4	3	2	1	BIT 0
	—	—	—	—	—	—	—	RAF
RESET:	0	0	0	0	0	0	0	0

Bits [7:1] — Not implemented
Always read zero

RAF — Receiver Active Flag (Read only)
0 = The receiver circuitry is idle
1 = A character is being received

SCDRH, SCDRL — SCI Data High, SCI Data Low **$102E, $102F**

	BIT 7	6	5	4	3	2	1	BIT 0	
$102E	R8	T8	—	—	—	—	—	—	High
$102F	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	Low

R8 — Receiver Bit 8
Ninth serial data bit received when SCI is configured for nine data bit operation (M = 1).

T8 — Transmitter Bit 8
Ninth serial data bit transmitted when SCI is configured for nine data bit operation (M = 1).

Bits [5:0] — Not implemented
Always read zero

R/T[7:0] — Receiver/Transmitter Data Bits 7 to 0
SCI data is double buffered in both directions.

9 Analog-to-Digital Converter

The analog-to-digital (A/D) converter system uses an all-capacitive charge-redistribution technique to convert analog signals to digital values. The MC68HC(7)11EA9 A/D converter system, a four-channel multiplexed-input successive-approximation converter, is accurate to ±1 least significant bit (LSB). It does not require external sample and hold circuits because of the type of charge-redistribution technique used.

Dedicated pins V_{RH} and V_{RL} provide the reference supply voltage inputs.

A multiplexer allows the single A/D converter to select one of 16 analog signals.

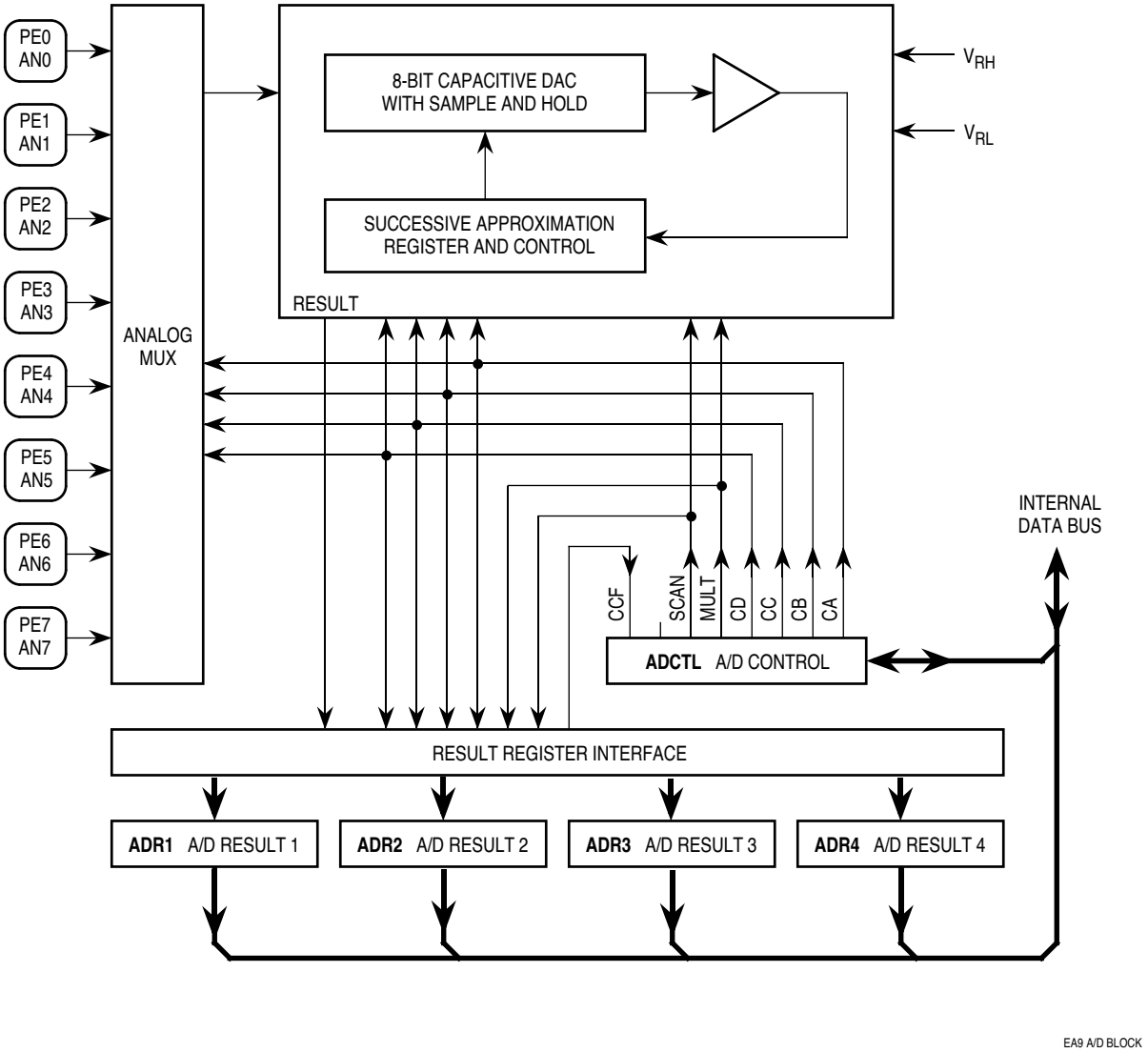


Figure 14 A/D Block Diagram

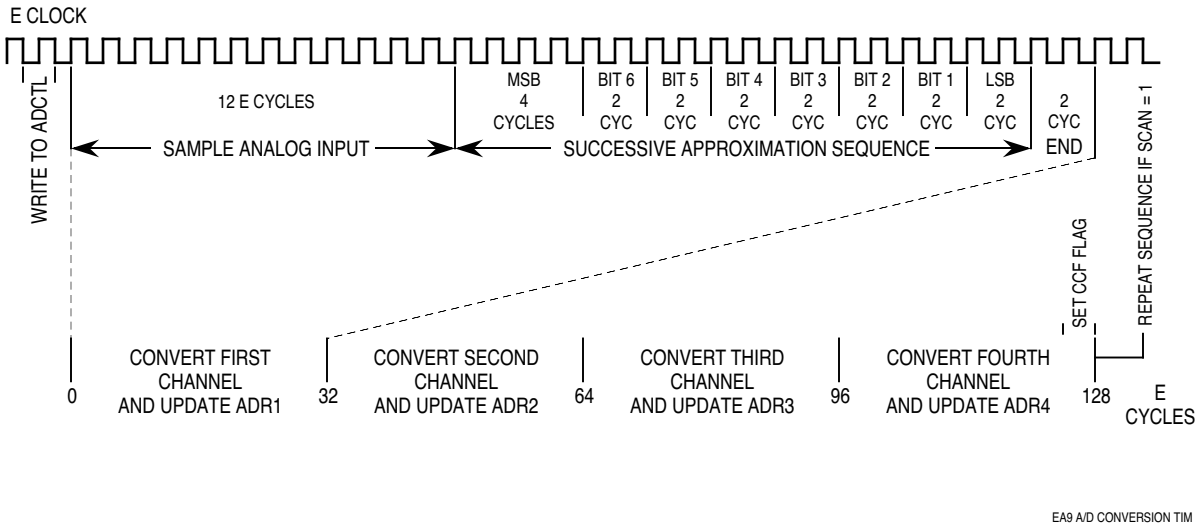


Figure 15 A/D Conversion Sequence

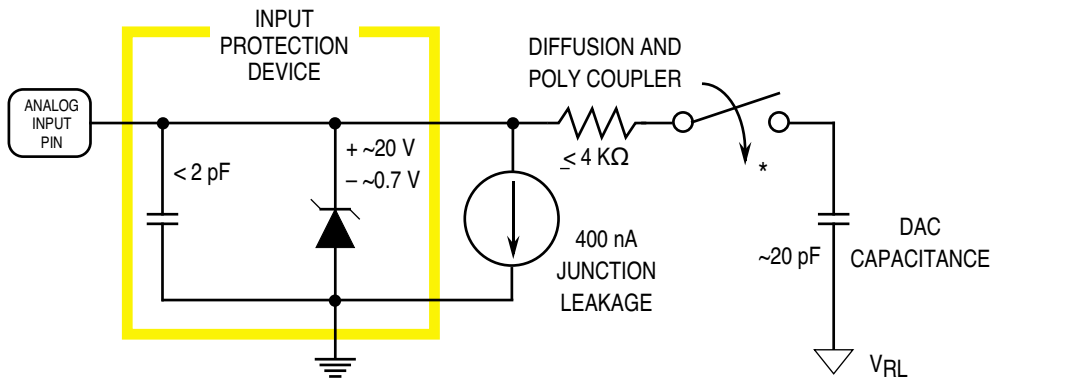


Figure 16 Electrical Model of an A/D Input Pin (Sample Mode)

ADCTL — A/D Control/Status **$1030**

	BIT 7	6	5	4	3	2	1	BIT 0
	CCF	—	SCAN	MULT	CD	CC	CB	CA
RESET:	I	0	I	I	I	I	I	I

CCF — Conversions Complete Flag

Set after an A/D conversion cycle is completed. CCF is cleared by a write to ADCTL.

0 = The A/D converter is currently performing a conversion sequence

1 = The A/D converter has completed a conversion, placed the result in the appropriate result register and is currently idle

Bit 6 — Not implemented

Always reads zero

SCAN — Continuous Scan Control

0 = Do four conversions and stop

1 = Convert four channels in selected group continuously

MULT — Multiple Channel/Single Channel Control

0 = Convert single channel selected

1 = Convert four channels in selected group

CD–CA — Channel Select D through A

Table 23 A/D Converter Channel Select Control Bits

Channel Select Control Bits				Channel	Result in ADRx if
CD	CC	CB	CA	Signal	MULT = 1
0	0	0	0	AN0	ADR1
0	0	0	1	AN1	ADR2
0	0	1	0	AN2	ADR3
0	0	1	1	AN3	ADR4
0	1	0	0	AN4	ADR1
0	1	0	1	AN5	ADR2
0	1	1	0	AN6	ADR3
0	1	1	1	AN7	ADR4
1	0	0	0	Reserved	—
1	0	0	1	Reserved	—
1	0	1	0	Reserved	—
1	0	1	1	Reserved	—
1	1	0	0	V_{RH}*	ADR1
1	1	0	1	V_{RL}*	ADR2
1	1	1	0	$(V_{RH})/2$*	ADR3
1	1	1	1	Reserved	ADR4

ADR1–ADR4 — A/D Results **$1031–$1034**

$1031	BIT 7	6	5	4	3	2	1	BIT 0	ADR1
$1032	BIT 7	6	5	4	3	2	1	BIT 0	ADR2
$1033	BIT 7	6	5	4	3	2	1	BIT 0	ADR3
$1034	BIT 7	6	5	4	3	2	1	BIT 0	ADR4

Table 24 Analog Input to 8-Bit Result Translation

	Bit 7	6	5	4	3	2	1	Bit 0
% (1)	50%	25%	12.5%	6.25%	3.12%	1.56%	0.78%	0.39%
VOLTS (2)	2.5	1.250	0.625	0.3125	0.1562	0.0781	0.0391	0.0195

(1) % of $V_{RH} - V_{RL}$ (2) Volts for $V_{RL} = 0$; $V_{RH} = 5.0$ V

OPTION — System Configuration Options **$1039**

	BIT 7	6	5	4	3	2	1	BIT 0
	ADPU	CSEL	IRQE*	DLY*	CME	—	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

* Can be written only once in first 64 cycles after reset in normal modes, or at any time in special modes.

ADPU — A/D Converter Power-Up
- 0 = A/D converter disabled and powered down
- 1 = A/D converter is enabled and powered on

CSEL — Clock Select
- 0 = A/D and EEPROM use the system E clock
- 1 = A/D and EEPROM use internal RC clock

IRQE — $\overline{\text{IRQ}}$ Select Edge-Sensitive Only
Refer to **5 Resets and Interrupts**.

DLY — Enable Oscillator Start-up Delay
- 0 = No stabilization delay on exit from STOP mode.
- 1 = A delay of approximately 4000 E-clock cycles is imposed as the MCU exits STOP mode.

CME — Clock Monitor Enable
Refer to **5 Resets and Interrupts**.

Bit 2 — Not implemented
Always reads zero

CR[1:0] — COP Timer Rate Select
Refer to **5 Resets and Interrupts**.

How to Reach Us:

Home Page:
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USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
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Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
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